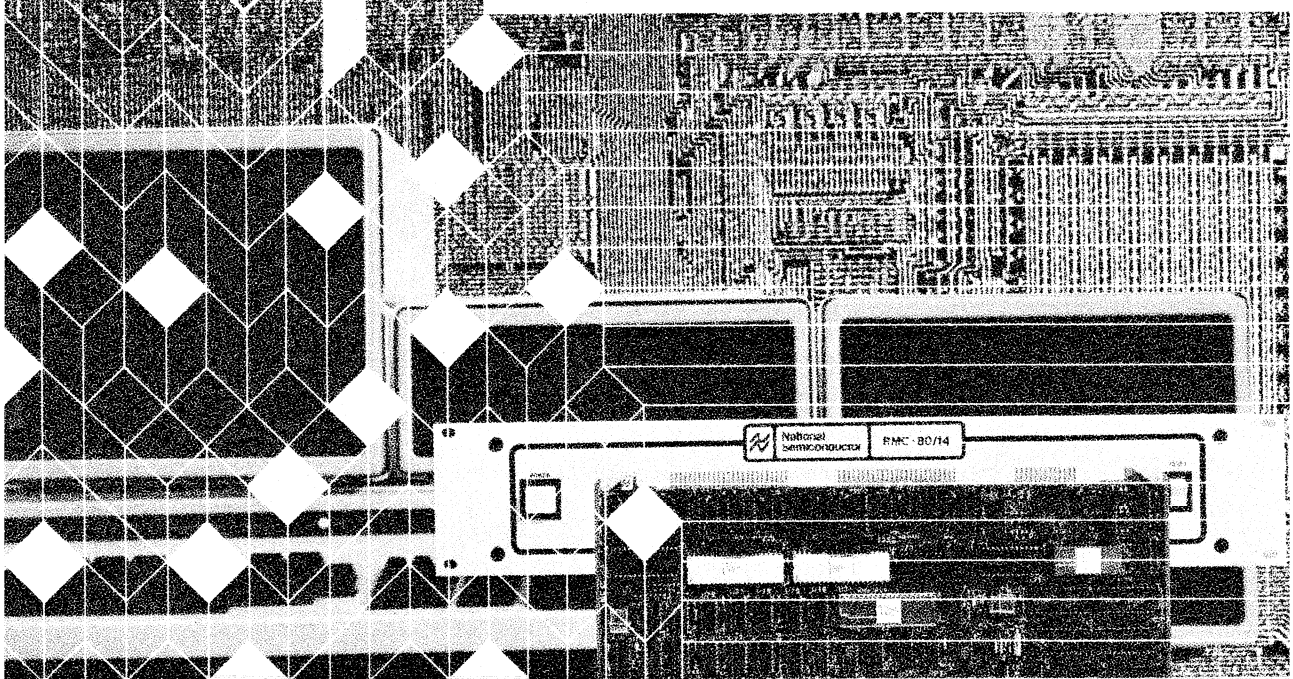
National Semiconductor Microcomputer Systems Series/80 Databook



January 1979

The National Series/80 Family

Introduction

The Series/80 product family from National Semiconductor provides a comprehensive base of Microcomputer Products. Fully compatible with the industry standard Series/80 architecture, many of these products are plug-for-plug, second source replacements for existing Intel* SBC products.

As well as being completely compatible with SBC products, National Series/80 products offer significant improvements such as greater reliability, more convenient user options, cleaner design and a full one year warranty. This saves the user design implementation time, lowers the cost of ownership and reduces inventory requirements.

Beyond providing a source for improved industry standard products, National's Series/80 family features proprietary products of totally new and differentiated design. As National's objective is to satisfy user demands, product engineers are allowed complete freedom to create new designs to meet the demands of the market. The STARPLEX™ Development System is one example of National's response to industry needs.

National's Series/80 family presently includes more than 50 individual computer products — everything needed to design advanced microcomputer systems.

This data book provides summary information on the complete line of board and system level microcomputer products. Also included is information about the National Semiconductor STARPLEX Development System. The National Series/80 product line is based around a broad series of Board Level Microcomputers. Each of these microcomputers is a complete system containing CPU, read/write memory, sockets for read only memory, parallel and serial I/O and bus interface circuitry on a single printed circuit board. These same CPU boards are also integrated into rack mountable computer (RMC) systems providing low cost packaged systems that include a microcomputer, power supply, card cage, chassis and front panel. Single board microcomputers and packaged systems are complemented by a wide variety of system expansion products including RAM and ROM/PROM memory, parallel and serial I/O, analog I/O, DMA and peripheral controllers. All of the National Semiconductor Series/80 products are compatible with the Intel MULTIBUS™ bus structure.

The National Semiconductor STARPLEX Development System supports the development of National microcomputer and microprocessor based products. Designed with the user's needs in mind, all the facilities necessary for the development of hardware and software packages are integrated into the STARPLEX system. Single-keystroke controls are provided for the software package that includes operating system, text editor, debugger, link editor, loader, file manager, macro assembler, FORTRAN, BASIC and many utility packages.

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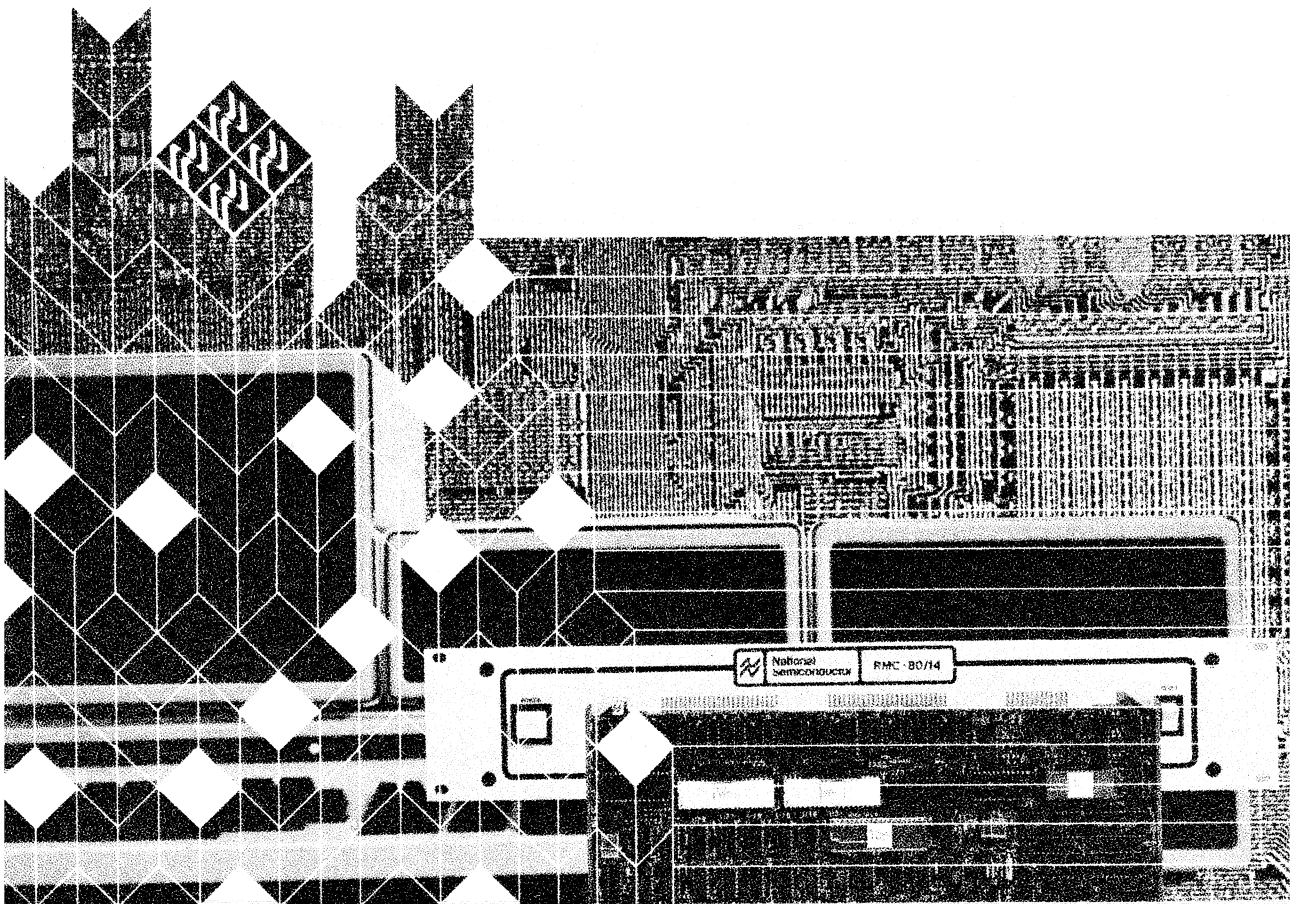
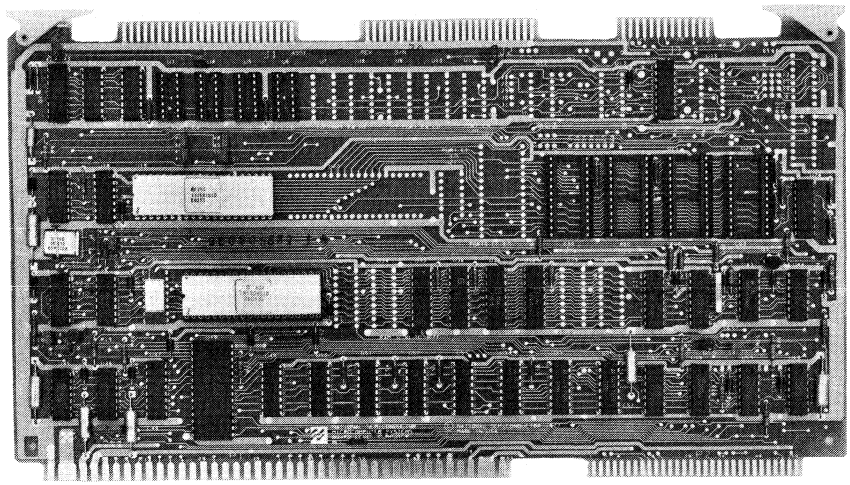
CPU Boards



National Semiconductor

BLC-80/07
Series/80 Board Level Computer



- **Low Cost with BLC/SBC-80/10 Computing Power**
- **24 Programmable Parallel I/O Lines — Fits Most Control Applications**
- **Less than 500 ns Memory Access Time for Fast Operation**
- **Compatible with BLC/SBC Series/80 Software and Hardware**
  - 8080A CPU
  - 4 Interrupt Lines
  - 512 Bytes of RAM
  - 4K Bytes of PROM
  - 64K Byte Addressing

Product Overview

The BLC-80/07 is a self-contained single board computer with the computing power of a BLC-80/10 computer. Based on the 8080A microprocessor, the BLC-80/07 is totally compatible with the wide range of BLC/SBC Series/80 hardware and software products.

The BLC-80/07 is a complete computer including a CPU, 24 parallel I/O lines, 512 bytes of static read write memory (RAM), sockets to accept 4K bytes of read only memory (ROM) and a system clock. The basic BLC-80/07 may be expanded in many dimensions through the addition of other products in the BLC/SBC Series/80 family, such as four slot chassis, power supply, RAM and ROM memory in any combination up to 64K bytes, various I/O controllers, digital and analog I/O, and other system modules.

The primary advantage of the BLC-80/07 is that it is a very low cost single board computer capable of solving a wide variety of applications problems, yet is expandable with standard Series/80 products at a reasonably low incremental cost.

Functional Description

Central Processor

- CPU: 8080A Microprocessor
- Maximum addressing range — 64K bytes
- Data word — 8 bits
- Instruction word — 8, 16 or 24 bits
- Addressing modes — direct, register, register indirect and immediate

- Instruction types — a total of 111
  - — 18 Data Transfer
  - — 29 Arithmetic
  - — 19 Logical
  - — 29 Branch
  - — 16 Control
- Registers
  - — 7 General Registers — 1 accumulator (A) plus six 8-bit work registers which may be utilized individually (B, C, D, E, H and L) or in pairs (B and C, D and E, H and L), effectively forming 16-bit registers.
  - — 1 16-bit Program Counter
  - — 1 16-bit Stack Pointer
  - — Sub-Routine Mechanism utilizes the stack pointer with push and pop instruction to implement "Call" and "Return" instruction types
- Sub-Routine Mechanism
  - — Hardware stack pointer with push and pop instructions
  - — Call and return instructions

Memory

512 bytes of static read write RAM is available on-board. The RAM is implemented using MM2111 memory modules. On-board memory addressing is predefined in the range 3E00 through 3FFF.

Sockets are installed on the computer to allow user implementation of read only memory for the specific application. The ROM section of the computer accepts 4K bytes of ROM using low cost MM2708 EPROM's. On-board ROM memory addressing is predefined in the range 0 through $0FFF_{16}$.

Memory expansion is possible using any mix of RAM and ROM memory expansion boards up to a maximum of 64K bytes. All expansion memory boards may be jumper selected for addressing in the range 0 through $FFFF_{16}$. This permits simple system integration.

Input/Output

The 24 input/output lines are controlled by an INS8255 Programmable Peripheral Interface circuit. Using standard Series/80 instructions, the 24 lines may be configured to a variety of unidirectional/bidirectional modes. The operating modes are defined in Appendix B.

- Interrupts
  - — 1 level with 4 individual lines
- Parallel
  - — 24 programmable I/O lines
  - — Latched, unlatched, strobed modes
  - — 8-bit parallel configuration
  - — Optional line drivers and terminators
  - — TTL compatible
- Compatible I/O Driver Modules
  - — A variety of driver circuit types are available for use in the input/output section: inverting, non-inverting, high voltage and open collector combinations with sink current capacity ranging from 16 to 48 milliamps.

(I = inverting; NI = non-inverting; OC = open collector; HV = high voltage)

Type	Output	Current (ma)
7438	I, OC, HV	48
7437	I	48
7432	NI	16
7426	I, OC, HV	16
7409	NI, OC	16
7408	NI	16
7403	I, OC	16
7400	I	16

- Compatible I/O Terminator Modules
  - — BLC-901 220/330 ohm divider
  - — BLC-902 1K ohm pull-up

System Bus

All address, data and control signals are TRI-STATE™ TTL compatible:

Type	Current (ma)
Address	50
Data	50
Control	32

The input/output section is specifically designed to permit the lines to be interfaced to a wide range of devices. Sockets are provided to allow matching line characteristics with driver and terminator circuits contained in 14 pin DIP packages. All drivers are TTL compatible. Two of the 3 parallel I/O ports are available for user implementation of appropriate driver circuits. Port number 1 has permanently installed 8226 type drivers.

National's BLC-901 and BLC-902 terminator modules are available as options to satisfy termination requirements. The BLC-901 contains 220/330 ohm divider type terminator circuits for four lines, while the BLC-902 contains 1K ohm pull-up type terminator circuits for four lines. Figure 1 illustrates the terminator circuit configuration.

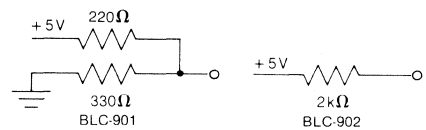


Figure 1. BLC-901 and BLC-902 Terminators

Interrupt

The CPU has a single level interrupt for recognition of events. Interrupts may originate from four sources OR-tied to the single level. When an interrupt is received, an in-process instruction is completed and then the program is suspended. The CPU passes control to a user defined interrupt service routine which saves system conditions while the interrupt is processed. Interrupt processing starts from location 0038_{16}.

Specifications

Microprocessor

CPU —	8080A (for Instruction Set, see Appendix A)
Data Word —	8 bits
Instruction Word —	8, 16 and 24 bits
Cycle Time —	1.95 microseconds (minimum instruction time)
System Clock —	2.048 MHz ± 0.1%
Registers —	6 General Purpose, 8-bit Accumulator, 8-bit Program Counter, 16-bit Stack Pointer, 16-bit
Number of Instructions —	111
Address Capacity —	64K bytes

Memory

RAM —	512 bytes on-board
ROM —	Sockets for 4K bytes on-board
Expansion —	Memory boards in any mix of RAM and ROM up to a 64K bytes maximum
Access Time —	500 nanoseconds (maximum)

Connectors

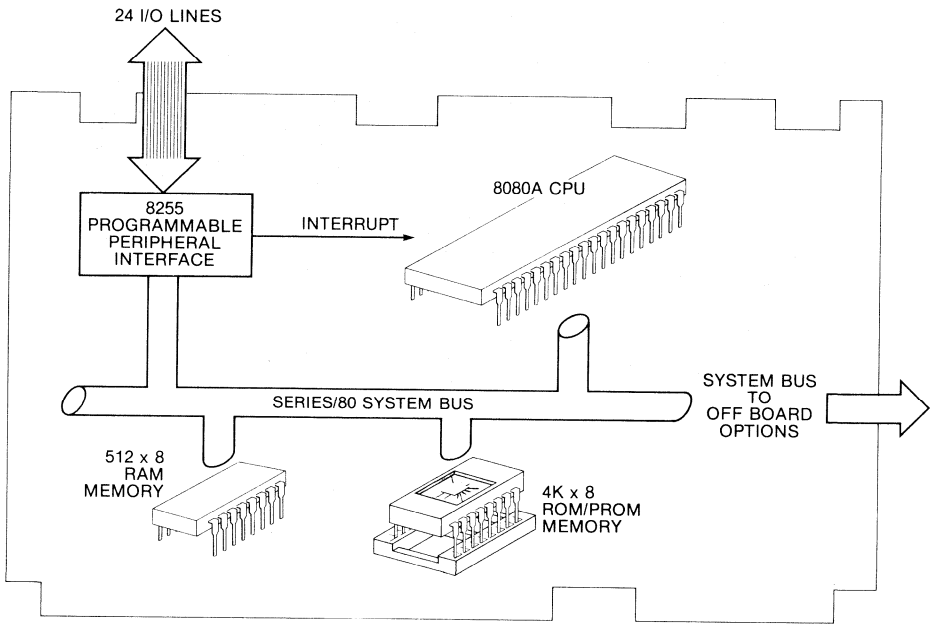
System Bus —	86 contact double-sided card cage edge connector on 0.156 inch centers
Auxiliary —	60 contact double-sided edge connector on 0.1 inch centers Recommended mating connector: CDC VPB01B30A00A2 AMP PES-14559 TI H311130
Parallel I/O —	50 contact double-sided edge connector on 0.1 inch centers Recommended mating connector: 3M 3415-0001 AMP 2-86792-3

Power	+5V, 2.2A −5V, 0.02A +12V, 0.15A −12V, 0.15A
Environmental	Temperature 0° to 55°C Humidity 0 to 90%, non-condensing

Physical	Height	6.75 in. (17.15 cm)
	Width	12.00 in. (30.48 cm)
	Depth	0.50 in. (1.27 cm)
	Weight	14 oz. (396.9 g)

Order Information

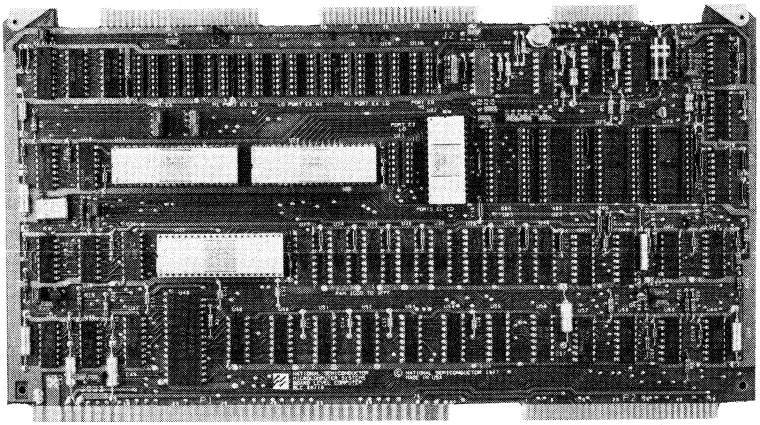
BLC-80/07	Series/80 Microcomputer Includes CPU, 512 bytes of static RAM, sockets for 4K bytes of ROM and 24 parallel I/O lines.



BLC-80/07 Diagram

National Semiconductor

BLC-80/10
Series/80 Board Level Computer



- **Low Cost Computing Power**
- **Compatible with Industry Standard BLC/SBC Series/80 Software and Hardware**
  - 8080A CPU
  - 6 interrupt sources
  - 1K static RAM
  - 4K ROM/PROM
- **48 Programmable Parallel I/O Lines to Fit Most Control and Data Interchange Applications**
- **Serial Communications Interface Configured for RS232C or 20 ma Current Loop**
- **Plug-replacement for Intel SBC-80/10**

Product Overview

The BLC-80/10 is a self contained Board Level Computer based on the INS8080A LSI microprocessor. The BLC-80/10 is functionally and physically compatible with the entire family of BLC/SBC hardware and software products.

The BLC-80/10 is a complete computer including a CPU, a serial communications interface, 48 parallel I/O lines, 1K bytes of static Random Access Memory (RAM), sockets to accept 4K bytes of Read Only Memory (ROM/PROM) and a system clock. The BLC-80/10 may be expanded beyond the basic system through the addition of other products in the BLC/SBC family such as a four or eight slot chassis, power supplies, RAM and ROM expansion in any combination up to 64K bytes, various I/O controllers, digital and analog I/O, and other system modules.

Functional Description

Central Processor

The INS8080A n-channel LSI microprocessor is the central processor for the BLC-80/10. The INS8080A contains six general purpose 8-bit registers, an 8-bit accumulator, a 16-bit stack pointer register, and a 16-bit program counter.

The six general purpose registers can be utilized singly or in pairs when double precision operations are required.

The 16-bit program counter allows direct addressing of a full 64K bytes of memory. The 16-bit stack pointer allows the user's stack to be located anywhere within the 64K memory space. This concept of locating a user's stack in system memory allows unlimited subroutine nesting levels and the flexibility of maintaining multiple stack areas.

Memory

The BLC-80/10 contains 1K bytes of on-board static RAM implemented with MM2111 memory modules. On-board memory addressing is predefined in the range $3C00_{16}$ to $3FFF_{16}$.

Sockets are installed to allow user implementation of read only memory for the specific application. Up to 4K bytes of ROM can be installed in 1K increments. MM2308 ROM's or low cost MM2708 EPROM's are acceptable devices. Addressing of the ROM/PROM's is predefined within the range 0000 to $0FFF_{16}$.

Memory expansion is possible using any mix of standard RAM and ROM expansion boards up to a maximum of 64K bytes. To provide simple system integration, all memory expansion boards can be jumper selected for addressing in the range 0000 through $FFFF_{16}$.

Input/Output

Parallel I/O

The 48 parallel input/output lines are controlled by two INS8255 Programmable Peripheral Interface (PPI) devices. Using standard Series/80 instructions, the 48 lines may be configured to a wide variety of unidirectional/bidirectional, latched/unlatched modes. The operating modes are defined in Appendix B.

The I/O section is specifically designed to permit the lines to be interfaced to a wide range of devices. Sockets are provided to allow matching line characteristics with driver and terminator circuits contained in 14-pin DIP packages. All parallel I/O lines are TTL compatible and are divided into six 8-bit ports. Five of the six parallel ports have provisions for user installed driver or terminator modules. Port 1 has permanently installed 8226 type drivers. Figure 1 illustrates the I/O address assigned to the 8255 PPI's.

	8255 No. 1				8255 No. 2			
Port	1	2	3	Control	4	5	6	Control
Address*	E4	E5	E6	E7	E8	E9	EA	EB

*Hexadecimal notation.

Figure 1. I/O Addresses

National's BLC-901 and BLC-902 terminator modules as well as a number of TTL devices are available to satisfy a variety of requirements. The BLC-901 contains 220/330 ohm divider type terminator circuits for four lines while the BLC-902 contains 1K ohm pull-ups for four lines. Figure 2 illustrates the terminator circuit configuration and Table 1 lists the compatible driver modules.

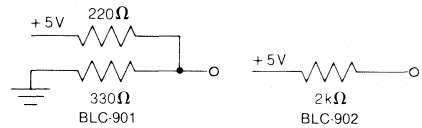


Figure 2. BLC-901 and BLC-902 Terminators

Table I. Compatible I/O Driver Modules

Type	Output	Current (ma)
7400	I	16
7403	I, OC	16
7408	NI	16
7409	NI, OC	16
7426	I, OC, HV	16
7432	NI	16
7437	I	48
7438	I, OC, HV	48

(I = inverting; NI = non-inverting; OC = open collector; HV = high voltage)

Serial I/O

One INS8251 Universal Synchronous/Asynchronous Receiver Transmitter (USART) provides the serial I/O port with programmable communications rates, data formats, control characters, and parity. Logic is provided for detection of framing, overrun, and parity errors as well as double buffering. The serial I/O port can be jumper selected to RS232C standards or 20 ma current loop, and interfaces via a 26-contact edge connector. Table 2 lists the serial baud rates available.

Table II. Serial Baud Rates

Baud Rate Clock (user selectable)	Baud Rate (Hz)		
	Synchronous	Asynchronous (program selectable)	
		÷16	÷64
307.2 KHz	—	19200	4800
153.6	—	9600	2400
76.8	—	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
3.49	3490	—	110

Interrupt System

The BLC-80/10 can handle 6 interrupt requests on a single interrupt level. Two are available for external user devices, one through the parallel I/O connector and one on the system bus. The remaining 4

interrupt sources are generated from on-board devices and are jumper selected. The on-board sources are as follows:

- 2 from the INS8255 PPI devices signifying input buffer full or output buffer empty
- 2 from the INS8251 USART device signifying input data ready or output character needed

The 6 interrupt sources share a common CPU level which causes a RESTART 7 instruction to be executed. The user response to the interrupt is handled by an interrupt processing routine starting at memory location 0038_{16}.

Specifications

Microprocessor

CPU —	INS8080A (for Instruction Set see Appendix A)
Data Word —	8 bits
Instruction Word —	8, 16, 24 bits
Cycle Time —	1.95 microseconds (minimum instruction time)
System Clock —	2.048 MHz ± 0.1%
Registers —	6 General Purpose, 8-bit Accumulator, 8-bit Program Counter, 16-bit Stack Pointer, 16-bit
Number of Instructions —	111
Address Capacity —	64K bytes

Memory

RAM —	1K bytes on-board
ROM —	Sockets for 4K bytes
Expansion —	Memory boards in any mix of RAM and ROM up to 64K bytes maximum
Access Time —	500 nanoseconds (maximum)

Input/Output

Interrupts —	Single level, 6 sources Programmable masking Active low TTL levels
Parallel —	48 lines Latched, unlatched, strobed modes 4- and 8-bit parallel configuration Optional line drivers and terminators TTL compatible
Serial —	20 ma current loop or RS232C
Synchronous Mode	5-8-bit character Internal/external synchronization Automatic SYNC insertion SYNC search
Asynchronous Mode	5-8-bit character 1, 1½, or 2 stop bits False start bit detect Break character generation

Connectors

System Bus —	86-contact double-sided card cage edge connector on 0.156-inch centers
Auxiliary —	60-contact double-sided edge connector on 0.1-inch centers Recommended mating connector: CDC VPB01B30A00A2 AMP PES-14559
Parallel I/O —	50-contact double-sided edge connector on 0.1-inch centers Recommended mating connector: 3M 3415-0001 AMP 2-86792-3
Serial I/O —	26-contact double-sided edge connector on 0.1-inch centers Recommended mating connector: 3M 3462-001 flat AMP 2-86792-3 round

Power

+5V, 2.9A
−5V, 0.002A
+12V, 0.14A
−12V, 0.18A
(excluding power required for I/O drivers and user supplied PROM's)

Environmental

Temperature 0° to 55°C
Humidity 0 to 90%
non-condensing

Physical

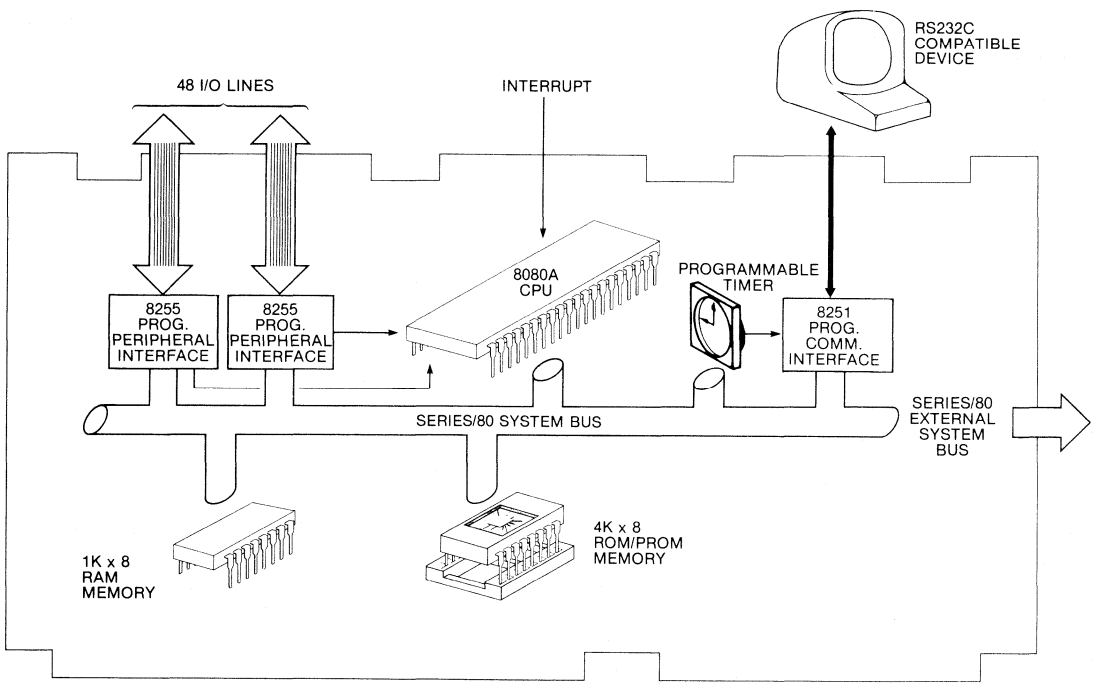
Height	6.75 in.	(17.15 cm)
Width	12.00 in.	(30.48 cm)
Depth	0.50 in.	(1.27 cm)
Weight	14 oz.	(396.9 g)

Order Information

BLC-80/10	Series/80 Microcomputer Includes CPU, 1K bytes of static RAM, sockets for 4K bytes of ROM, 48 parallel I/O lines and a serial communications interface.

Documentation

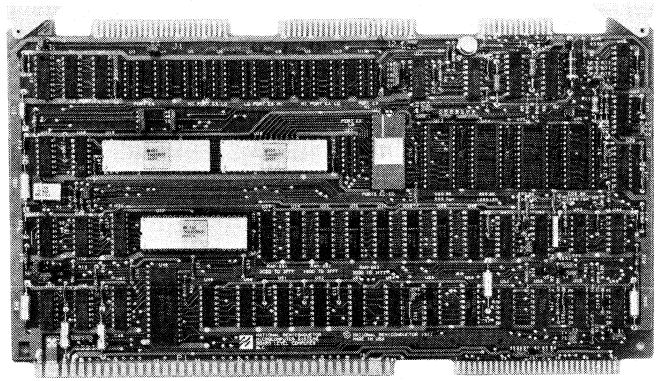
420305373-001	BLC-80/10 Board Level Computer Hardware Reference Manual



BLC-80/10 Diagram

National Semiconductor

BLC-80/11, BLC-80/12, BLC-80/14 Series/80 Board Level Computer



- **Low Cost Computing Power with Expanded On-Board Memory**
- **Compatible with Industry Standard BLC/SBC Series/80 Software and Hardware**
  - 8080A CPU
  - 6 interrupt sources
  - 1K, 2K, 4K static RAM
  - UP TO 8K ROM/PROM
- **48 Programmable I/O Lines to Fit Most Control and Data Interchange Applications**
- **Serial Communications Interface Configured for RS232C or 20 ma Current Loop**
- **RS232C Interface Selectable for Data Set or Data Terminal**
- **Plug-replacement for Intel SBC-80/10A**

Product Overview

The BLC-80/11, 80/12, and 80/14 are self contained Board Level Computers based on the INS8080A LSI microprocessor. These computers are functionally and physically compatible with the entire family of BLC/SBC hardware and software products.

The BLC-80/11, 80/12, and 80/14 are complete computers including a CPU, a serial communications interface, 48 parallel I/O lines, up to 4K bytes of static Random Access Memory (RAM), sockets to accept up to 8K bytes of Read Only Memory (ROM/PROM) and a system clock. These computers may be expanded beyond the basic system through the addition of other products in the BLC/SBC family such as a four or eight slot chassis, power supplies, RAM and ROM expansion in any combination up to 64K bytes, various I/O controllers, digital and analog I/O, and other system modules.

The primary advantage of the BLC-80/11, 80/12, and 80/14 over the BLC-80/10 is their increased RAM and ROM capacity.

Functional Description

Central Processor

The INS8080A n-channel LSI microprocessor is the central processor for the BLC-80/11, 80/12, and 80/14. The INS8080A contains six general purpose 8-bit registers, an 8-bit accumulator, a 16-bit stack pointer register, and a 16-bit program counter.

The six general purpose registers can be utilized singly or in pairs when double precision operations are required.

The 16-bit program counter allows direct addressing of a full 64K bytes of memory. The 16-bit stack pointer allows the user's stack to be located anywhere within the 64K memory space. This concept of locating a user's stack in system memory allows unlimited subroutine nesting levels and the flexibility of maintaining multiple stack areas.

Memory

The BLC-80/11, 80/12 and 80/14 contain 1K, 2K, or 4K bytes, respectively, of on-board static RAM implemented with MM2111 memory modules. On-board memory addressing is predefined in the range 3000_{16} to $3FFF_{16}$, depending upon the amount of RAM installed.

Four sockets are installed to allow user implementation of read only memory for the specific application. Jumpers are provided to allow the use of MM2308/MM2316E ROM's or MM2708/MM2716 EPROM's, giving a total of 8K bytes of read only memory in 1K or 2K increments. Addressing of the ROM/PROM's is predefined within the range 0000 to $0FFF_{16}$ or $1FFF_{16}$, depending upon the type of ROM installed.

Memory expansion is possible using any mix of standard RAM and ROM expansion boards up to a maximum of 64K bytes. To provide simple system integration, all memory expansion boards can be jumper selected for addressing in the range 0000 through $FFFF_{16}$.

Input/Output

Parallel I/O

The 48 parallel input/output lines are controlled by two INS8255 Programmable Peripheral Interface (PPI) devices. Using standard Series/80 instructions, the 48 lines may be configured to a wide variety of unidirectional/bidirectional, latched/unlatched modes. The operating modes are defined in Appendix B.

The I/O section is specifically designed to permit the lines to be interfaced to a wide range of devices. Sockets are provided to allow matching line characteristics with driver and terminator circuits contained in 14-pin DIP packages. All parallel I/O lines are TTL compatible and are divided into six 8-bit ports. Five of the six parallel ports have provisions for user installed driver or terminator modules. Port 1 has permanently installed 8226 type drivers. Figure 1 illustrates the I/O address assigned to the 8255 PPI's.

	8255 No. 1				8255 No. 2			
Port	1	2	3	Control	4	5	6	Control
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*Hexadecimal notation.

Figure 1. I/O Addresses

National's BLC-901 and BLC-902 terminator modules as well as a number of TTL devices are available to satisfy a variety of requirements. The BLC-901 contains 220/330 ohm divider type terminator circuits for four lines while the BLC-902 contains 1K ohm pull-ups for four lines. Figure 2 illustrates the terminator circuit configuration and Table 1 lists the compatible driver modules.

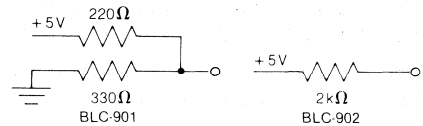

Figure 2. BLC-901 and BLC-902 Terminators

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7426	I, OC, HV	16
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7437	I	48
7438	I, OC, HV	48

(I = inverting; NI = non-inverting; OC = open collector; HV = high voltage)

Serial I/O

One INS8251 Universal Synchronous/Asynchronous Receiver Transmitter (USART) provides the serial I/O port with programmable communications rates, data formats, control characters, and parity. Logic is provided for detection of framing, overrun, and parity errors as well as double buffering. The serial I/O port can be jumper selected to RS232C standards or 20 ma current loop, and interfaces via a 26-contact edge connector. Table 2 lists the serial baud rates available.

Table II. Serial Baud Rates

Baud Rate Clock (user selectable)	Baud Rate (Hz)		
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76.8	—	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
3.49	3490	—	110

Interrupt System

The BLC-80/11, 80/12, and 80/14 can handle 6 interrupt requests on a single interrupt level. Two are available for external user devices, one through the parallel I/O connector and one on the system bus. The remaining 4 interrupt sources are generated from on-board devices and are jumper selected. The on-board sources are as follows:

- 2 from the INS8255 PPI devices signifying input buffer full or output buffer empty
- 2 from the INS8251 USART device signifying input data ready or output character needed

The 6 interrupt sources share a common CPU level which causes a RESTART 7 instruction to be executed. The user response to the interrupt is handled by an interrupt processing routine starting at memory location 0038_{16}.

Specifications

Microprocessor

CPU —	INS8080A (for Instruction Set see Appendix A)
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Cycle Time —	1.95 microseconds (minimum instruction time)
System Clock —	2.048 MHz ± 0.1%
Registers —	6 General Purpose, 8-bit Accumulator, 8-bit Program Counter, 16-bit Stack Pointer, 16-bit
Number of Instructions —	111
Address Capacity —	64K bytes

Memory

RAM —	BLC-80/11	1K bytes
	BLC-80/12	2K bytes
	BLC-80/14	4K bytes
ROM —	Sockets for up to 8K bytes	
RAM Memory Addressing —	BLC-80/11	$3C00_{16}$ to $3FFF_{16}$
	BLC-80/12	3800_{16} to $3FFF_{16}$
	BLC-80/14	3000_{16} to $3FFF_{16}$
ROM Memory Addressing —	0000 to $0FFF_{16}$ or $1FFF_{16}$	
Expansion —	Memory boards in any mix of RAM and ROM up to 64K bytes maximum	
Access Time —	500 nanoseconds (maximum)	

Input/Output

Interrupts —	Single level, 6 sources Programmable masking Active low TTL levels
Parallel —	48 lines Latched, unlatched, strobed modes 4- and 8-bit parallel configuration Optional line drivers and terminators TTL compatible
Serial —	20 ma current loop or RS232C
Synchronous Mode	5-8-bit character Internal/external synchronization Automatic SYNC insertion SYNC search
Asynchronous Mode	5-8-bit character 1, 1½, or 2 stop bits False start bit detect Break character generation

Connectors

System Bus —	86-contact double-sided card cage edge connector on 0.156-inch centers
Auxiliary —	60-contact double-sided edge connector on 0.1-inch centers Recommended mating connector: CDC VPB01B30A00A2 AMP PES-14559
Parallel I/O —	50-contact double-sided edge connector on 0.1-inch centers Recommended mating connector: 3M 3415-0001 AMP 2-86792-3
Serial I/O —	26-contact double-sided edge connector on 0.1-inch centers Recommended mating connector: 3M 3462-001 flat AMP 2-86792-3 round

Power

+5V, 2.9A
−5V, 0.002A
+12V, 0.14A
−12V, 0.18A
(excluding power required for I/O drivers and user supplied PROM's)

Environmental

Temperature 0° to 55°C
Humidity 0 to 90%
non-condensing

Physical

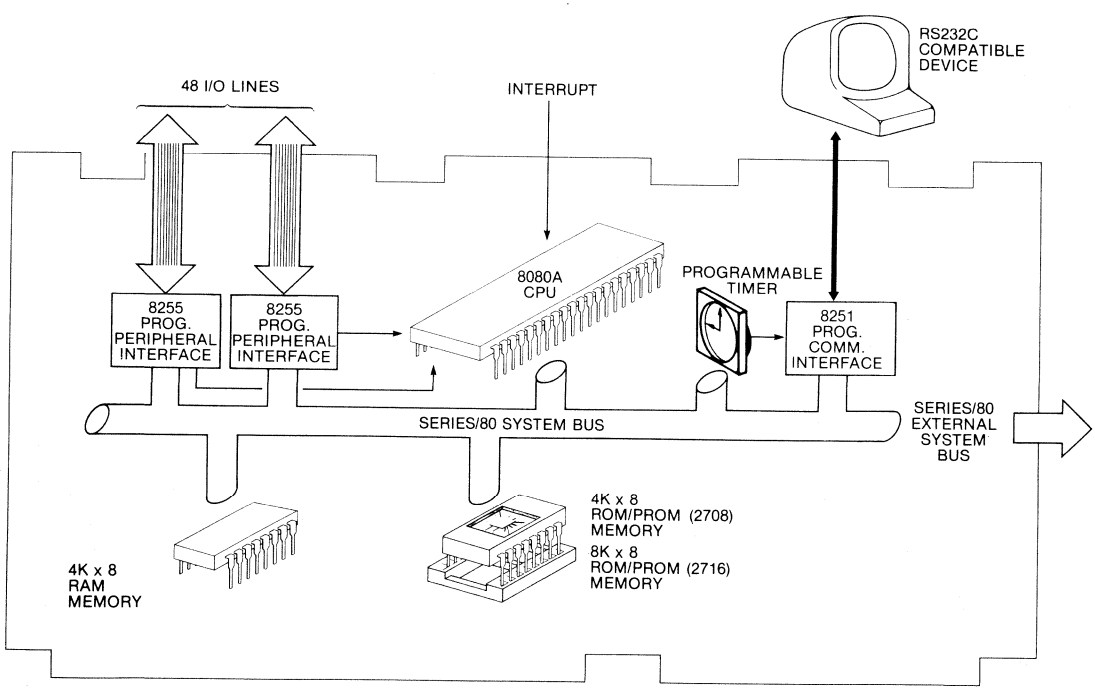
Height	6.75 in.	(17.15 cm)
Width	12.00 in.	(30.48 cm)
Depth	0.50 in.	(1.27 cm)
Weight	14 oz.	(396.9 g)

Order Information

BLC-80/11	Series/80 Microcomputer Includes CPU, 1K bytes of static RAM, sockets for 4K or 8K bytes of ROM, 48 parallel I/O lines and a serial communications interface.
BLC-80/12	Series/80 Microcomputer Includes CPU, 2K bytes of static RAM, sockets for 4K or 8K bytes of ROM, 48 parallel I/O lines, and a serial communications interface.
BLC-80/14	Series/80 Microcomputer Includes CPU, 4K bytes of static RAM, sockets for 4K or 8K bytes of ROM, 48 parallel I/O lines, and serial communications interface.

Documentation

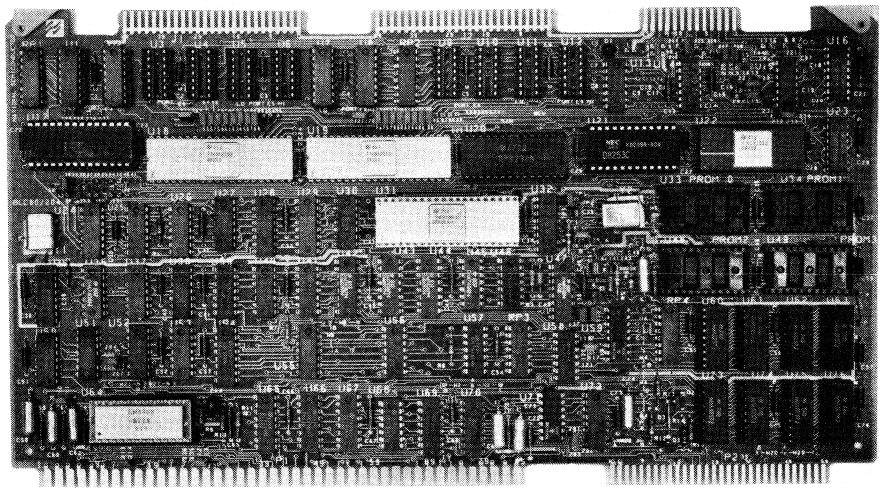
420305532-001	BLC-80/11, 80/12, 80/14 Board Level Computer Hardware Reference Manual



BLC-80/14 Diagram

National Semiconductor

BLC-80/204
Series/80 Board Level Computer



- **Complete System Capability, including:**
  - 8 vectored interrupts
  - Multiple processor capability — up to six bus masters
  - Interval timer with three programmable counters
  - ROM/RAM "shadowing" capability under software control
  - Larger memory — 4K bytes RAM and sockets for up to 8K bytes of EPROM/ROM
  - Programmable RS232C communications interface with program selectable baud rates
- **Low Power MM5257 Static RAM with Battery Backup Circuitry**
- **Fully Compatible with Industry Standard BLC/SBC Series/80 Family of Microcomputer Products**
- **Plug-for-Plug Compatible with the Intel SBC-80/20 and SBC-80/204**

Product Overview

The BLC-80/204 is a self-contained board level computer with 4K bytes RAM. System features on the BLC-80/204 allow building more complex and powerful systems including multi-processor configurations. Based upon the 8080A-2 microprocessor, the BLC-80/204 incorporates special Series/80 bus arbitration logic to sort out contention disputes among several processors sharing the same system bus.

Minicomputer systems concepts widely accepted among computer systems builders, such as vectored interrupts, have been incorporated into the BLC-80/204. Vectored interrupts is a hardware technique that automatically handles all the necessary details of identifying the interrupts, storing the status of the CPU, and initiating the interrupt service routine. This technique is superior to the software polling scheme of non-vectored CPU's since it eliminates unnecessary cycling through a software polling routine to determine which interrupt to service.

Microcomputer industry concepts, such as a single chip Universal Synchronous/Asynchronous Receiver/Transmitter (USART), are included. The USART features include a vast number of transmission rates, from 110 to 38,400 baud, all under program control.

The BLC-80/204 is a complete computer including:

- CPU
- Serial I/O
- Parallel I/O
- Interval timers
- Vectored interrupts
- RAM and ROM memory

The basic BLC-80/204 microcomputer can be expanded by the addition of a four slot chassis, power supply, ROM and RAM memory, various I/O controllers, analog and digital I/O and other system modules — even more BLC-80/204's. Thus, the basic advantage of the BLC-80/204 is that it provides low cost single board computer capability, yet is expandable to a substantially more powerful multiprocessor configuration.

Functional Description

Central Processor

- CPU: 8080A-2 Microprocessor
- Maximum addressing range — 64K bytes
- Data word — 8 bits
- Instruction word — 8, 16, 24 bits
- Addressing modes — direct, register, register indirect and immediate
- Instruction types — total of 111 instructions
  - — 18 data transfer
  - — 29 arithmetic
  - — 19 logical
  - — 29 branch
  - — 16 central
- Registers
  - — 7 general registers — 1 accumulator (A) plus six 8-bit work registers which may be utilized individually (B, C, D, E, H, L) or in pairs (B and C, D and E, H and L), effectively forming three 16-bit registers.
  - — 1 16-bit program counter.
  - — 1 16-bit stack pointer.
- Subroutine mechanism
  - — Hardware stack pointer with push and pop instruction
  - — Call and return instructions

Memory

- 4K bytes of static read/write memory using MM5257 RAM with auxiliary battery backup power bus (160 ma, 1.5 V)
- Sockets on-board for up to 8K bytes of ROM in 1K or 2K increments using MM2708 or MM2716 EPROM
- Memory expansion to 64K bytes using any combination of RAM/ROM memory boards
- A memory shadow technique is incorporated allowing on-board ROM memory addresses to be identical to off-board ROM/RAM memory addresses. By switching back and forth via software, a ROM bootstrap routine can "disappear" from memory to be replaced with RAM once the system start-up procedure is past the bootstrap stage.
- On-board RAM memory addressing in the range 2000_{16} through $FFFF_{16}$ selectable on 4K byte boundaries. Off-board RAM memory addressing from 0000 to $FFFF_{16}$.
- ROM/PROM memory addressing in the range 0000 through $1FFF_{16}$.
- An automatic synchronizing signal is generated by the processor during non-memory access time periods to allow the off-board dynamic RAM expansion memory to go through a refresh cycle without reducing system throughput. This unique refresh synchronizing technique effectively allows the dynamic expansion memory to exhibit static memory characteristics.

Input/Output

- Parallel I/O
  - — Two INS8255 programmable peripheral interface circuits provide a total of 48 I/O lines which can be configured by software into any combination of unidirectional/bidirectional I/O ports. Sockets are provided on the board to allow selection of drivers and terminators appropriate for each application. All I/O lines are interfaced using a pair of 50 contact edge connectors for mating with cables. The operating modes are defined in Appendix B.
- Serial I/O
  - — One INS8251 Universal Synchronous/Asynchronous Receiver/Transmitter provides the serial I/O port with programmable communications rates, data formats, control characters and parity. Logic is provided for detection of framing, overrun and parity errors, as well as double buffering. The serial I/O port provides RS232C signals interfaced via a 26 contact edge connector.

Interval Timer (Clocks)

Three programmable 16-bit counters are included. One is used as a baud rate generator for the serial I/O port and the other two are used as general

purpose BCD or binary 16-bit counters. The other two can be cascaded into one 32-bit counter. Each clock has up to seven software selectable functions:

- Interrupt on termination of a specified count
- Programmable one-shot
- Rate generator based upon a multiple of the input clock period
- Square wave rate generator
- Software triggered strobe
- Hardware triggered strobe
- Event counter (using external signal to drive clock input)

Input Frequencies —	Reference 1.0752 MHz ± 0.1% Event rate 1.1 MHz maximum
Output Frequencies/ Timing Intervals —	Variable time intervals from 1.86 microseconds to 1.109 hours. Frequency variation from 25 KHz to 537.61 KHz.

Interrupt System

A programmable interrupt module handles interrupt vectoring of eight interrupt levels. Four priority processing modes may be reconfigured under program control during system operation. Interrupts in any combination may be masked under program control.

The programmable interrupt module accepts interrupts from parallel and serial I/O, programmable timers, or the system bus. Each interrupt is serviced based on its priority, which is determined by attaching the device interrupt line to one of eight system bus interrupt lines.

Each of the eight BLC-80/204 levels is connected to a specific line on the system bus. Each level may be connected to as many as 16 interrupts, but the system will not detect more than one interrupt at a time on the same level. A software polling routine may be used to distinguish among multiple interrupts on the same level if more than eight are desired. On-board interrupt sources are available as follows:

4 — two from each of two 8255 parallel I/O modules

2 — two from the 8251 serial I/O module

2 — one from each of two available system clocks

Interrupts may come from up to 8 sources on the Series/80 system bus and up to 48 from the I/O ports on the two 8255's.

A block of memory (32 or 64 bytes) must be reserved for interrupt vectors. The address for each level is spaced at intervals of 4 or 8 bytes (program selectable). A single JUMP instruction at each location links the ultimate service routine.

Expansion to 64 levels of vectored interrupts is possible using off-board logic.

Table 1. Programmable Interrupt Modes

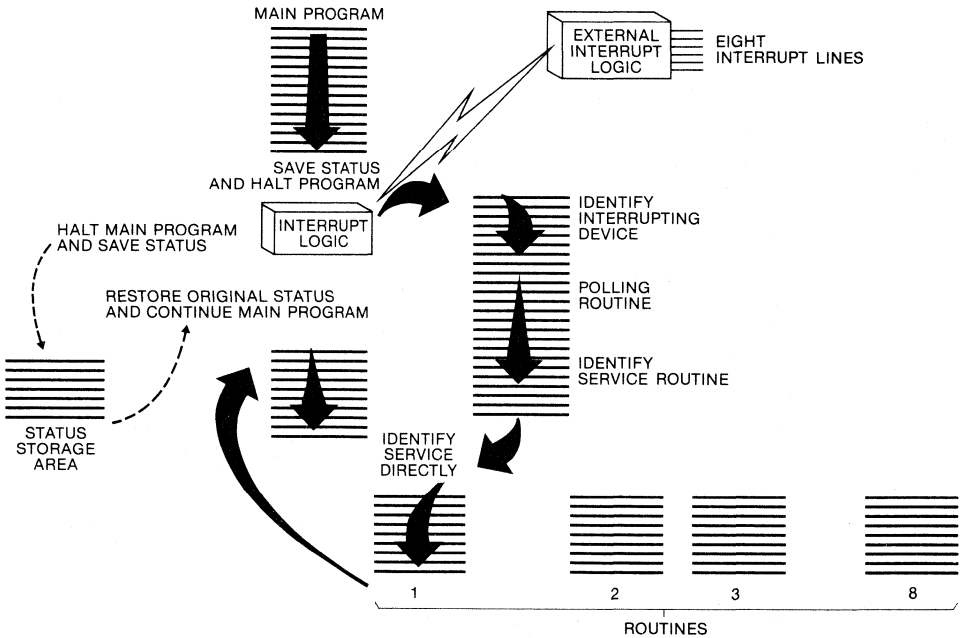
Mode	Operation
Fully Nested	Interrupt request line priorities fixed at 0 (highest) through 7 (lowest).
Auto-Rotating	Once serviced, a given level becomes the lowest priority level until the next interrupt occurs.
Specific Priority	Software assigns the lowest priority level.
Polled	Software examines an interrupt status by using the interrupt status register.

System Bus Arbitration

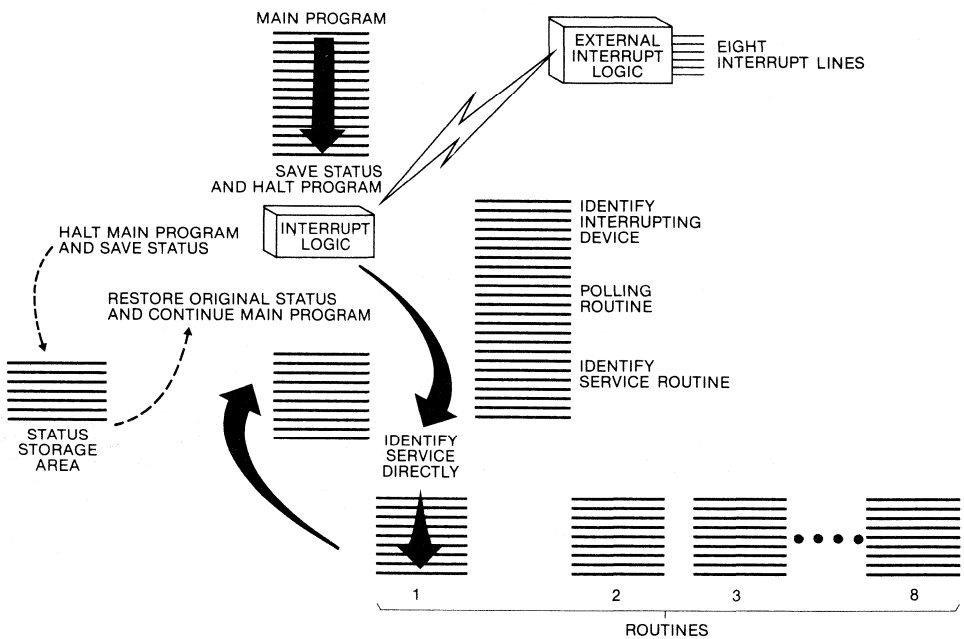
The Series/80 system bus allows multiple devices to transfer data on a common bus.

The Series/80 system bus allows multiprocessing. Each bus master attached to the Series/80 system bus must provide multi-master bus arbitration logic to prevent contention errors. When used in a system configuration, bus arbitration logic elements on each of the bus masters are interconnected to form a dynamic master/slave relationship.

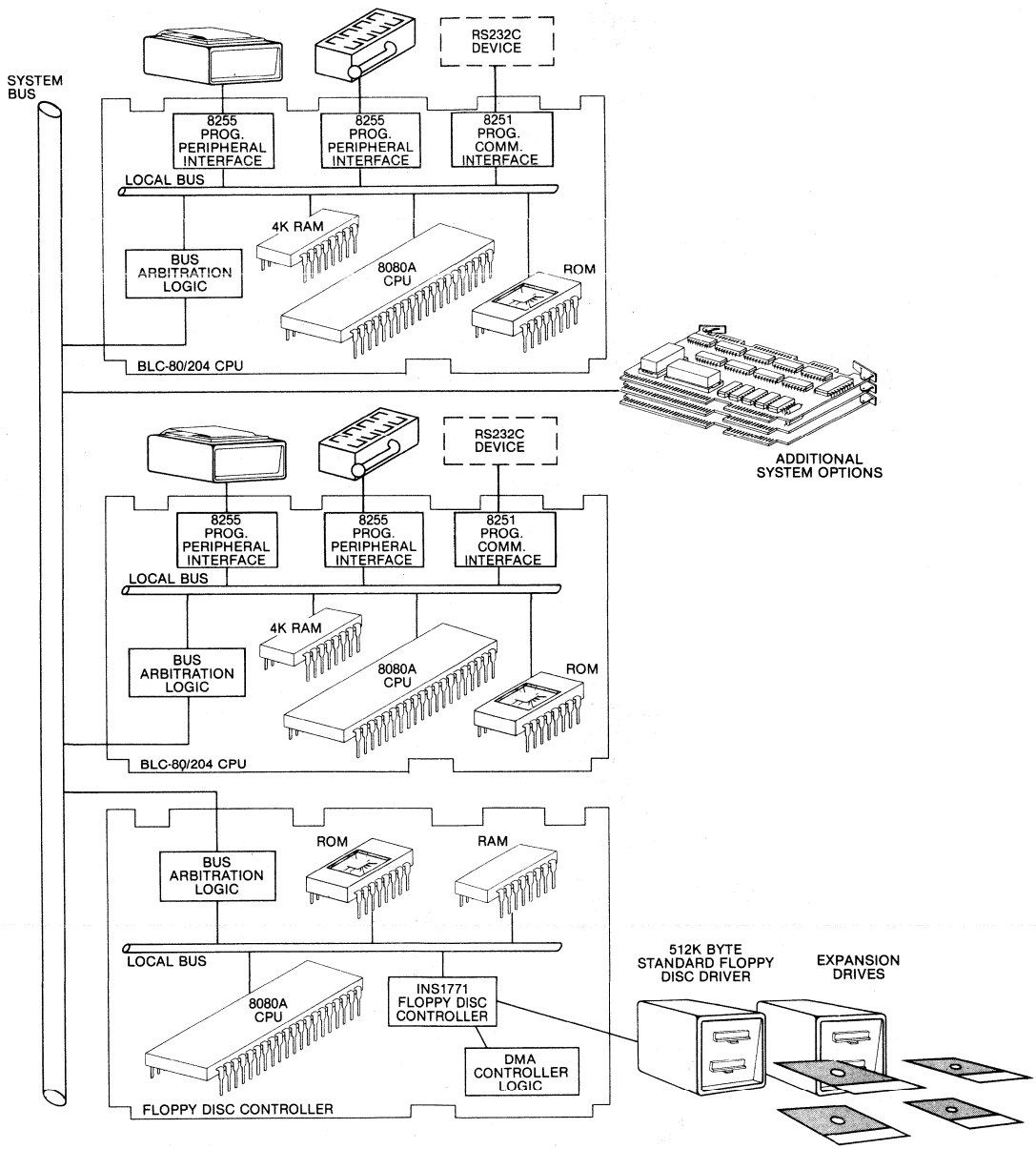
The bus arbitration logic modules can be connected in a straight-line priority scheme where bus control is granted in daisy-chaining fashion from the highest priority to the lowest priority. Any bus master taking control of the bus thereby denies it to bus masters lower in priority in the chain. Using the straight-line priority scheme, there may be up to six bus masters on a single system. By using off-board logic, as many as sixteen bus masters are possible.



Without Vectored Interrupts



Vectored Interrupts



Typical Microprocessor: BLC-80/204 System Diagram

Specifications

Microprocessor

CPU —	8080A-2 (for Instruction Set, see Appendix A)
Data Word —	8 bits
Instruction Word —	8, 16 and 24 bits
Cycle Time —	1.86 microseconds (minimum instruction time)
System Clock —	2.1504 MHz ± 0.1%
Registers —	6 General Purpose, 8-bit Accumulator, 8-bit Program Counter, 16-bit Stack Pointer, 16-bit
Number of Instructions —	111
Address Capacity —	64K bytes

Memory

RAM —	4K bytes on-board
ROM —	Sockets for 4K bytes on-board (ROM/PROM/EPROM)
Expansion —	Memory boards in any mix of RAM and ROM up to a 64K byte maximum
Access Time —	500 nanoseconds (maximum)

Input/Output

Interrupts —	8 level hardware vectored interrupts Programmable masking 4 priority modes
Parallel —	48 programmable I/O lines Latched, unlatched, strobed modes 4- and 8-bit parallel configuration Optional line drivers and terminators TTL compatible

Compatible I/O Driver Modules
(I = inverting; NI = non-inverting; OC = open collector; HV = high voltage)

Type	Output	Current (ma)
7438	I, OC, HV	48
7437	I	48
7432	NI	16
7426	I, OC, HV	16
7409	NI, OC	16
7408	NI	16
7403	I, OC	16
7400	I	16

Compatible I/O Terminator Modules —	BLC-901 220/330 ohm divider BLC-902 1K ohm pull-up
Serial —	Programmable Full data set control Double buffered RS232C compatible Synchronous mode: 5-8-bit character Internal/external synchronization Automatic SYNC insertion SYNC search 75-9600 baud Asynchronous mode: 5-8-bit character 1, 1½ or 2 stop bits False start bit detect 1760-38400 baud Break character generation
System Bus	Multiple bus master capability for up to 6 masters, expandable to 16 masters with additional priority network. All address, data and control signals are TRI-STATE™ TTL compatible:

Type	Current (ma)
Address	50
Data	50
Control	32

Interval Timer (Clocks)

Clocks —	3 programmable
Size —	16 bits
Interval —	1.86 microseconds to 1.109 hours
Frequency Variation —	25 KHz to 537.61 KHz

Connectors

System Bus — 86 contact double-sided card cage edge connector on 0.156 inch centers

Auxiliary — (Battery back-up) 60 contact double-sided edge connector on 0.1 inch centers

Recommended mating connector:
CDC VPB01B30A00A2
AMP PES-14559
TI H311130

Parallel I/O — 50 contact double-sided edge connector on 0.1 inch centers

Recommended mating connector:
3M 3415-0001
AMP 2-86792-3

Serial I/O — 26 contact double-sided edge connector on 0.1 inch centers

Recommended mating connector:
3M 3462-0001 flat
AMP 1-583715-1 round

Power

VDC	Normal	Battery
+5V	4.9A	0.36A
−5V	0.18A	—
+12V	0.35A	—
−12V	0.02A	—

(normal based on 4K ROM installed)

Environmental Temperature 0° to 55°C
Humidity 0 to 90%, non-condensing

Physical

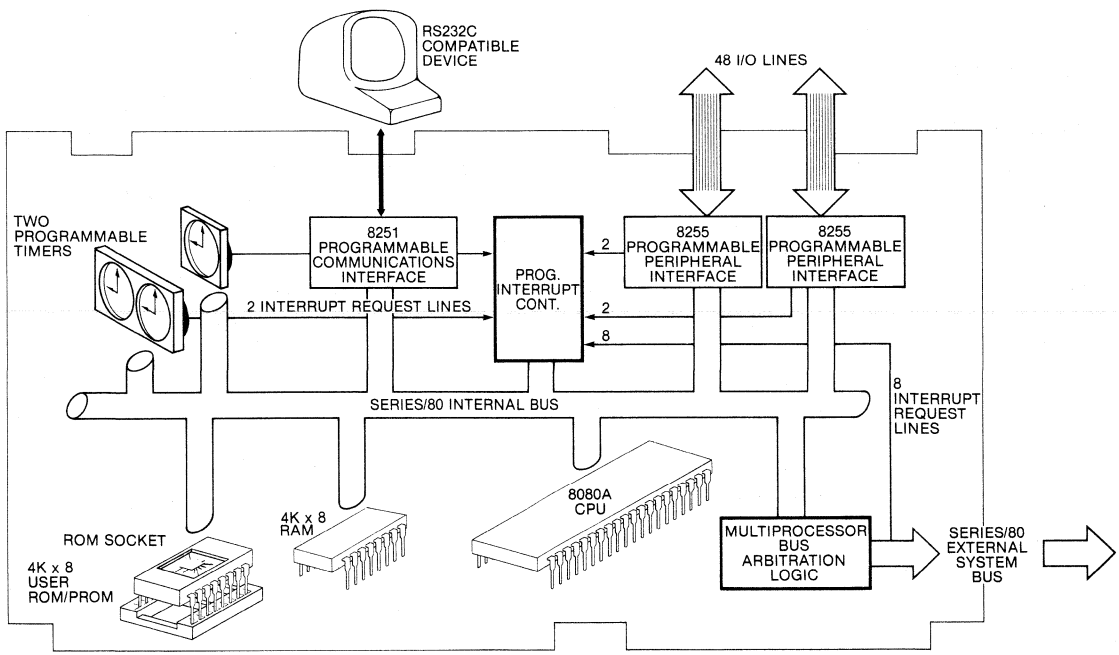
Height	6.75 in.	(17.15 cm)
Width	12.00 in.	(30.48 cm)
Depth	0.50 in.	(1.27 cm)
Weight	14 oz.	(396.9 g)

Order Information

BLC-80/204 Series/80 Microcomputer Includes CPU, 4K bytes of static RAM, sockets for 8K bytes of ROM, 48 parallel I/O lines and an RS232C serial I/O

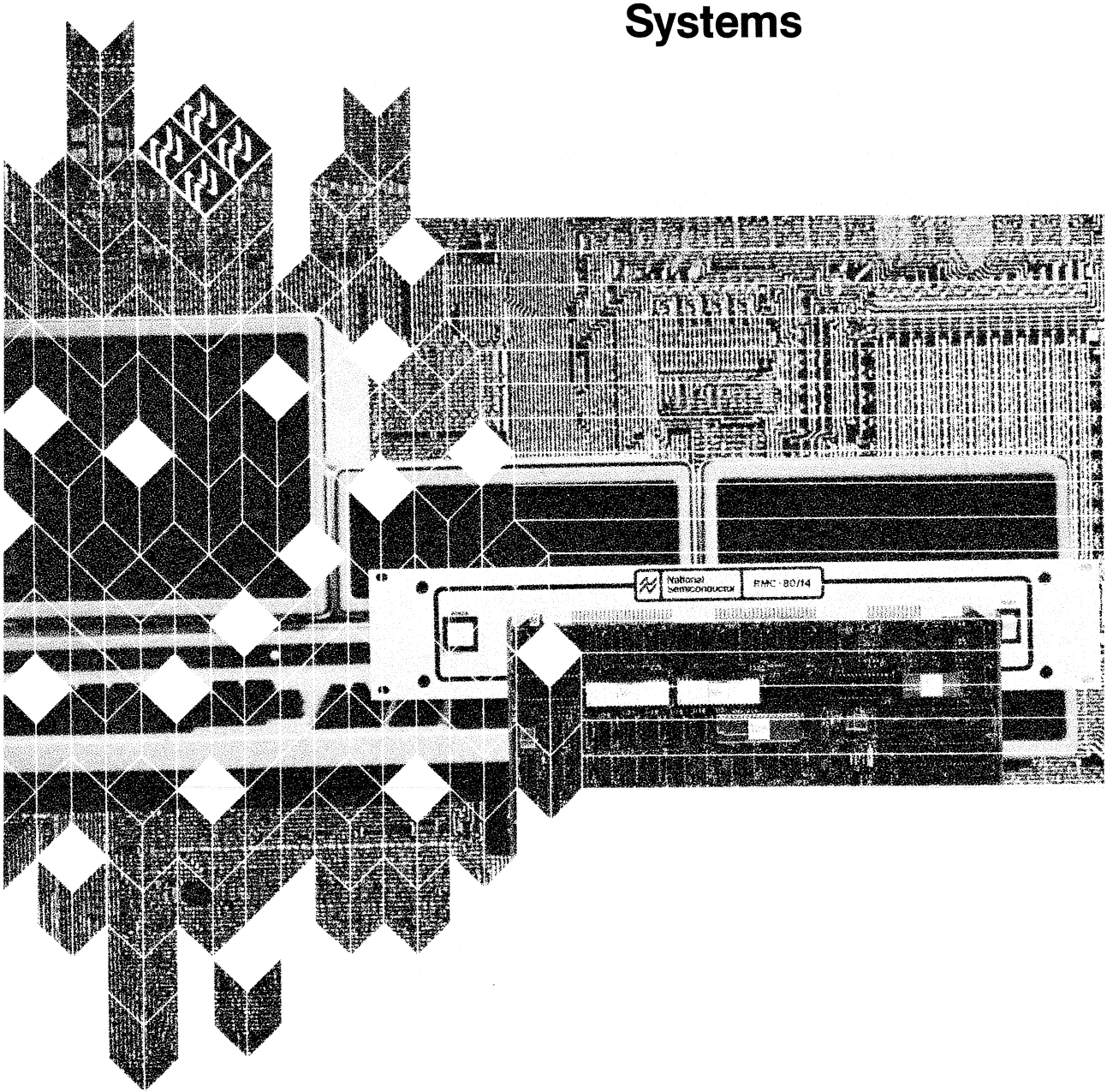
Documentation

420305521-001 BLC-80/204 Board Level Computer Hardware Reference Manual

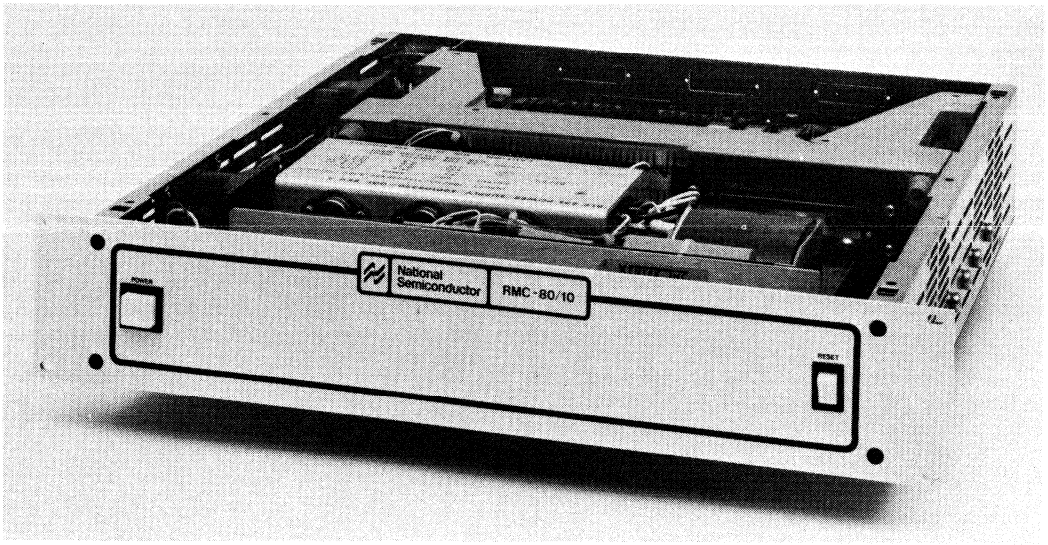


BLC-80/204 Diagram

Section 2
Rack Mountable Microcomputer Systems



RMC-80/10
Rack Mountable Computer



- **Fully Self-Contained Rack Mountable Package for OEM Applications**
  - BLC-80/10 Board Level Computer
  - BLC-910 System Monitor for loading, executing, debugging programs
  - BLC-635 Power Supply
  - BLC-604 4-Slot Card Cage
- **Front Panel with Power and Reset Switches**
- **Rear Panel with D Type Connector Knockouts**
- **Expandable with Standard BLC/SBC Series/80 Products**
- **Replacement for Intel's System 80/10**

Product Overview

The RMC-80/10 is a packaged microcomputer system based on the BLC-80/10 Board Level Computer. The RMC-80/10 occupies only 3½ inches of vertical space in a standard 19-inch RETMA rack. The self-contained power supply has enough capacity to handle the BLC-80/10 CPU board plus three additional expansion boards. The 3½-inch chassis contains the CPU board, power supply, fans, and three expansion board slots.

The CPU board in the RMC-80/10 is based on the INS8080A LSI microprocessor. The RMC-80/10 is functionally compatible with the entire family of BLC/SBC hardware and software products.

Installed in the RMC-80/10 is a complete Board Level Computer including a CPU, a serial communications interface, 48 parallel I/O lines, 1K bytes of static Random Access Memory (RAM), sockets to accept 4K bytes of Read Only Memory (ROM/PROM) and a system clock. The RMC-80/10 may be expanded beyond the basic system through the addition of other products in the BLC/SBC family such as RAM and ROM expansion boards in any combination up to 64K bytes, various I/O controllers, digital and analog I/O, and other system modules.

Functional Description

BLC-80/10 CPU

The INS8080A n-channel LSI microprocessor is the central processor for the BLC-80/10. The INS8080A contains six general purpose 8-bit registers, an 8-bit accumulator, a 16-bit stack pointer register, and a 16-bit program counter.

The six general purpose registers can be utilized singly or in pairs when double precision operations are required.

The 16-bit program counter allows direct addressing of a full 64K bytes of memory. The 16-bit stack pointer allows the user's stack to be located anywhere within the 64K memory space. This concept of locating a user's stack in system memory allows unlimited subroutine nesting levels and the flexibility of maintaining multiple stack areas.

Memory

The BLC-80/10 contains 1K bytes of on-board static RAM implemented with MM2111 memory modules. On-board memory addressing is predefined in the range $3C00_{16}$ to $3FFF_{16}$.

Sockets are installed to allow user implementation of read only memory for the specific application. Up to 4K bytes of ROM can be installed in 1K increments. MM2308 ROM's or low cost MM2708 EPROM's are acceptable devices. Addressing of the ROM/PROM's is predefined within the range 0000 to $0FFF_{16}$.

Memory expansion is possible using any mix of standard RAM and ROM expansion boards up to a maximum of 64K bytes. To provide simple system integration, all memory expansion boards can be jumper selected for addressing in the range 0000 through $FFFF_{16}$.

Input/Output

Parallel I/O

The 48 parallel input/output lines are controlled by two INS8255 Programmable Peripheral Interface (PPI) devices. Using standard Series/80 instructions, the 48 lines may be configured to a wide variety of unidirectional/bidirectional, latched/unlatched modes. The operating modes are defined in Appendix B.

The I/O section is specifically designed to permit the lines to be interfaced to a wide range of devices. Sockets are provided to allow matching line characteristics with driver and terminator circuits contained in 14-pin DIP packages. All parallel I/O lines are TTL compatible and are divided into six 8-bit ports. Five of the six parallel ports have provisions for user installed driver or terminator modules. Port 1 has permanently installed 8226 type drivers. Figure 1 illustrates the I/O addresses assigned to the 8255 PPI's.

	8255 No. 1				8255 No. 2			
Port	1	2	3	Control	4	5	6	Control
Address*	E4	E5	E6	E7	E8	E9	EA	EB

*Hexadecimal notation.

Figure 1. I/O Addresses

National's BLC-901 and BLC-902 terminator modules as well as a number of TTL devices are available to satisfy a variety of requirements. The BLC-901 contains 220/330 ohm divider type terminator circuits for four lines while the BLC-902 contains 1K ohm pull-ups for four lines. Figure 2 illustrates the terminator circuit configuration and Table 1 lists the compatible driver modules.

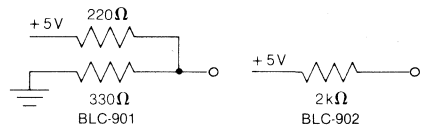


Figure 2. BLC-901 and BLC-902 Terminators

Table I. Compatible I/O Driver Modules

Type	Output	Current (ma)
7400	I	16
7403	I, OC	16
7408	NI	16
7409	NI, OC	16
7426	I, OC, HV	16
7432	NI	16
7437	I	48
7438	I, OC, HV	48

(I = inverting; NI = non-inverting; OC = open collector; HV = high voltage)

Serial I/O

One INS8251 Universal Synchronous/Asynchronous Receiver Transmitter (USART) provides the serial I/O port with programmable communications rates, data formats, control characters, and parity.

Logic is provided for detection of framing, overrun, and parity errors as well as double buffering. The serial I/O port can be jumper selected to RS232C standards or 20 ma current loop, and interfaces via a 26-contact edge connector. In the RS232C mode, jumper selection is available to reconfigure the port as either a data set or a data terminal. Table 2 lists the serial baud rates available.

Table II. Serial Baud Rates

Timer Selection	Baud Rate Clock (user selectable software)	Baud Rate (Hz)		
		Synchronous	Asynchronous (program selectable)	
			÷16	÷64
÷7	153.6 KHz	—	9600	2400
÷14	76.8 KHz	—	4800	1200
÷28	38.4 KHz	38400	2400	600
÷56	19.2 KHz	19200	1200	300
÷112	9.6 KHz	9600	600	150
÷224	4.8 KHz	4800	300	75
÷448	2.4 KHz	2400	150	
÷611	1.76 KHz	1760	110	

Interrupt System

The BLC-80/10 can handle 6 interrupt requests on a single interrupt level. Two are available for external user devices, one through the parallel I/O connector and one on the system bus. The remaining 4 interrupt sources are generated from on-board devices and are jumper selected. The on-board sources are as follows:

- 2 from the INS8255 PPI devices signifying input buffer full or output buffer empty
- 2 from the INS8251 USART device signifying input data ready or output character needed

The 6 interrupt sources share a common CPU level which causes a RESTART 7 instruction to be executed. The user response to the interrupt is handled by an interrupt processing routine starting at memory location 0038_{16}.

BLC-910 System Monitor Firmware

Two MM2708 PROM's containing the system monitor are installed in the BLC-80/10. The monitor can be used for loading, debugging, and executing programs. Also available are commands to read and punch paper tape, execute program segments, and display and alter memory locations and CPU registers. The Hardware Reference Manual supplied with the RMC-80/10 contains a source listing of the system monitor. This listing allows the user to execute existing routines by using CALL and JUMP instructions.

The system monitor permits the insertion of breakpoints to facilitate software and hardware debugging and contains the following commands:

D Display Memory
G Execute Program
I Insert into Memory
M Move Memory
R Read Hexadecimal File
S Substitute Memory
W Write Hexadecimal File
X Examine and Modify Registers
B Write BNPF File

Specifications

Refer to specifications for BLC-80/10, BLC-604, and BLC-635.

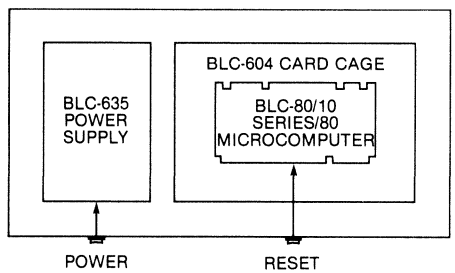
Front Panel Switches —	Power On/Off Reset		
System Monitor —	Addresses $0000-0506_{16}$ (ROM) $3C00-3C3F_{16}$ (RAM)		
Input Power —	100, 115, 215, 230 VAC ± 10% 47-63 Hz		
DC Power Available for Expansion Boards —	+12V, 1.6A +5V, 10.0A −5V, 0.9A −12V, 0.625A Assumes fully loaded CPU board with PROM's and terminators installed.		
Environmental —	Temperature 0° to 55°C Humidity 0 to 90% non-condensing		
Physical —	Height	3.5 in.	(8.89 cm)
	Width	19 in.	(48.26 cm)
	Depth	20 in.	(50.8 cm)
	Weight	37 lb.	(16.8 kg)

Order Information

RMC-80/10	Rack Mountable Computer System, 110-115 VAC, 60 Hz
RMC-80/10E	Rack Mountable Computer System, 200-230 VAC, 50 Hz
	Both systems include: BLC-80/10 CPU board, BLC-635 Power Supply, BLC-910 System Monitor, a 115 volt power cable, 115 volt and 230 volt fuses, dual fans, 3 expansion slots, operator panel and documentation.

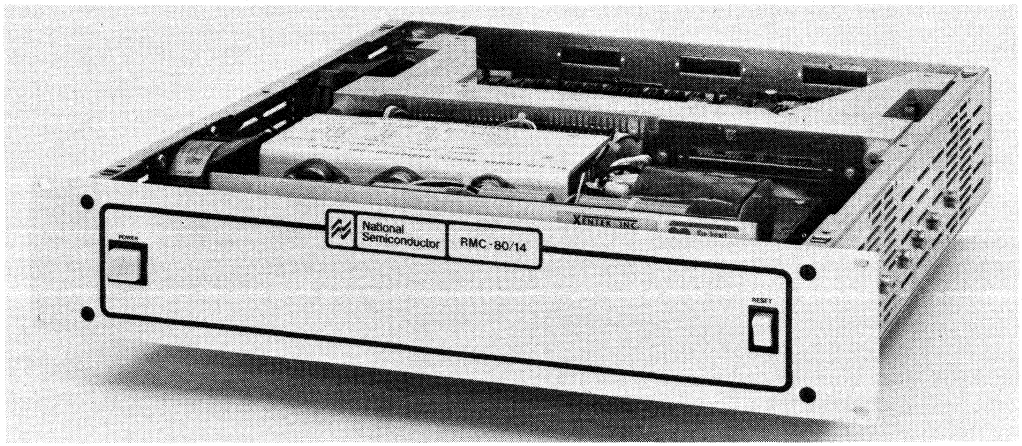
Documentation

420305535-001	RMC-80/10 Enclosure Monitor User's Manual
420305506-001	RMC-80/10 Rack Mountable Computer Hardware Reference Manual (3 manual set)
420305388-001	BLC-80P Prototyping Package User's Manual
420305489-001	BLC-635 Power Supply User's Manual



RMC-80/10 Diagram

RMC-80/14
Rack Mountable Computer



- **Fully Self-Contained Rack Mountable Package for OEM Applications**
  - BLC-80/14 Board Level Computer
  - BLC-910 System Monitor for loading, executing, debugging programs
  - BLC-635 Power Supply
  - BLC-604 4-Slot Card Cage
- **Front Panel with Power and Reset Switches**
- **Rear Panel with Provision for User Installed Connectors**
- **Expandable with Standard BLC/SBC Series/80 Products**

Product Overview

The RMC-80/14 is a packaged microcomputer system based on the BLC-80/14 Board Level Computer. The RMC-80/14 occupies only 3½ inches of vertical space in a standard 19-inch RETMA rack. The self-contained power supply has enough capacity to handle the BLC-80/14 CPU board plus three additional expansion boards. The chassis contains the CPU board, power supply, fans, and three expansion board slots.

The CPU board in the RMC-80/14 is based on the INS8080A LSI n-channel microprocessor. The RMC-80/14 is functionally compatible with the entire family of BLC/SBC hardware and software products.

Installed in the RMC-80/14 is a BLC-80/14 Board Level Computer including a CPU, a serial communications interface, 48 parallel I/O lines, 4K bytes of static Random Access Memory (RAM), sockets to accept up to 8K bytes of Read Only Memory (ROM/PROM) and a system clock. The RMC-80/14 may be expanded beyond the basic system through the addition of other products in the BLC/SBC family such as RAM and ROM expansion boards in any combination up to 64K bytes, various I/O controllers, digital and analog I/O, and other system modules.

Functional Description

BLC-80/14 CPU

The INS8080A n-channel LSI microprocessor is the central processor for the BLC-80/14 CPU. The INS8080A contains six general purpose 8-bit registers, an 8-bit accumulator, a 16-bit stack pointer register, and a 16-bit program counter.

The six general purpose registers can be utilized singly or in pairs when double precision operations are required.

The 16-bit program counter allows direct addressing of a full 64K bytes of memory. The 16-bit stack pointer allows the user's stack to be located anywhere within the 64K memory space. This concept of locating a user's stack in system memory allows unlimited subroutine nesting levels and the flexibility of maintaining multiple stack areas.

Memory

The BLC-80/14 contains 4K bytes of on-board static RAM implemented with MM2111 memory modules. On-board memory addressing is predefined in the range 3000_{16} to $3FFF_{16}$, depending on the type of ROM installed.

Sockets are installed on the BLC-80/14 to allow user implementation of read only memory for the specific application. Up to 8K bytes of ROM can be installed in 1K or 2K increments. MM2308/MM2316E ROM's or low cost MM2708/MM2716 EPROM's are acceptable devices. Addressing of the ROM/PROM's is predefined within the range 0000 to $0FFF_{16}$ or $1FFF_{16}$, depending on the type of ROM installed.

Memory expansion is possible using any mix of standard RAM and ROM expansion boards up to a maximum of 64K bytes. To provide simple system integration, all memory expansion boards can be jumper selected for addressing in the range 0000 through $FFFF_{16}$.

Input/Output

Parallel I/O

The 48 parallel input/output lines are controlled by two INS8255 Programmable Peripheral Interface (PPI) devices. Using standard Series/80 instructions, the 48 lines may be configured to a wide variety of unidirectional/bidirectional, latched/unlatched modes. The operating modes are defined in Appendix B.

The I/O section is specifically designed to permit the lines to be interfaced to a wide range of devices. Sockets are provided to allow matching line characteristics with driver and terminator circuits contained in 14-pin DIP packages. All parallel I/O lines are TTL compatible and are divided into six 8-bit ports. Five of the six parallel ports have provisions for user installed driver or terminator modules. Port 1 has permanently installed 8226 type drivers. Figure 1 illustrates the I/O addresses assigned to the 8255 PPI's.

	8255 No. 1				8255 No. 2			
Port	1	2	3	Control	4	5	6	Control
Address*	E4	E5	E6	E7	E8	E9	EA	EB

*Hexadecimal notation.

Figure 1. I/O Addresses

National's BLC-901 and BLC-902 terminator modules as well as a number of TTL devices are available to satisfy a variety of requirements. The BLC-901 contains 220/330 ohm divider type terminator circuits for four lines while the BLC-902 contains 1K ohm pull-ups for four lines. Figure 2 illustrates the terminator circuit configuration and Table 1 lists the compatible driver modules.

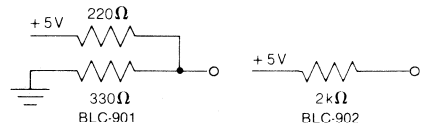


Figure 2. BLC-901 and BLC-902 Terminators

Table I. Compatible I/O Driver Modules

Type	Output	Current (ma)
7400	I	16
7403	I, OC	16
7408	NI	16
7409	NI, OC	16
7426	I, OC, HV	16
7432	NI	16
7437	I	48
7438	I, OC, HV	48

(I = inverting; NI = non-inverting; OC = open collector; HV = high voltage)

Serial I/O

One INS8251 Universal Synchronous/Asynchronous Receiver Transmitter (USART) provides the serial I/O port with programmable communications rates, data formats, control characters, and parity. Logic is provided for detection of framing, overrun, and parity errors as well as double buffering. The serial I/O port can be jumper selected to RS232C standards or 20 ma current loop, and interfaces via a 26-contact edge connector. In the RS232C mode, jumper selection is available to reconfigure the port as either a data set or a data terminal. Table 2 lists the serial baud rates available.

Table II. Serial Baud Rates

Timer Selection	Baud Rate Clock (user selectable software)	Baud Rate (Hz)		
		Synchronous	Asynchronous (program selectable)	
			÷16	÷64
÷7	153.6 KHz	—	9600	2400
÷14	76.8 KHz	—	4800	1200
÷28	38.4 KHz	38400	2400	600
÷56	19.2 KHz	19200	1200	300
÷112	9.6 KHz	9600	600	150
÷224	4.8 KHz	4800	300	75
÷448	2.4 KHz	2400	150	
÷611	1.76 KHz	1760	110	

Interrupt System

The BLC-80/14 can handle 6 interrupt requests on a single interrupt level. Two are available for external user devices, one through the parallel I/O connector and one on the system bus. The remaining 4 interrupt sources are generated from on-board devices and are jumper selected. The on-board sources are as follows:

- 2 from the INS8255 PPI devices signifying input buffer full or output buffer empty
- 2 from the INS8251 USART device signifying input data ready or output character needed

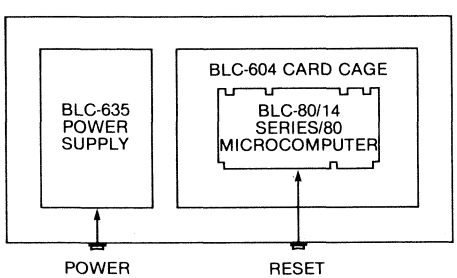
The 6 interrupt sources share a common CPU level which causes a RESTART 7 instruction to be executed. The user response to the interrupt is handled by an interrupt processing routine starting at memory location 0038_{16}.

BLC-910 System Monitor Firmware

Two MM2708 PROM's containing the system monitor are installed in the BLC-80/14. The monitor can be used for loading, debugging, and executing programs. Also available are commands to read and punch paper tape, execute program segments, and display and alter memory locations and CPU registers. The Hardware Reference Manual supplied with the RMC-80/14 contains a source listing of the system monitor. This listing allows the user to execute existing routines by using CALL and JUMP instructions.

The system monitor permits the insertion of breakpoints to facilitate software and hardware debugging and contains the following commands:

D	Display Memory
G	Execute Program
I	Insert into Memory
M	Move Memory
R	Read Hexadecimal File
S	Substitute Memory
W	Write Hexadecimal File
X	Examine and Modify Registers
B	Write BNPF File



RMC-80/14 Diagram

Specifications

Refer to specifications for BLC-80/14, BLC-604, and BLC-635.

Front Panel Switches —	Power On/Off Reset	
System Monitor —	Addresses $0000-0506_{16}$ (ROM) $3C00-3C3F_{16}$ (RAM)	
Input Power —	100, 115, 215, 230 VAC ± 10% 47-63 Hz	
DC Power Available for Expansion Boards —	+12V, 1.6A +5V, 10.0A −5V, 0.9A −12V, 0.625A Assumes fully loaded CPU board with PROM's and terminators installed.	
Environmental —	Temperature 0° to 55°C Humidity 0 to 90% non-condensing	
Physical —	Height	3.5 in. (8.89 cm)
	Width	19 in. (48.26 cm)
	Depth	20 in. (50.8 cm)
	Weight	37 lb. (16.8 kg)

Order Information

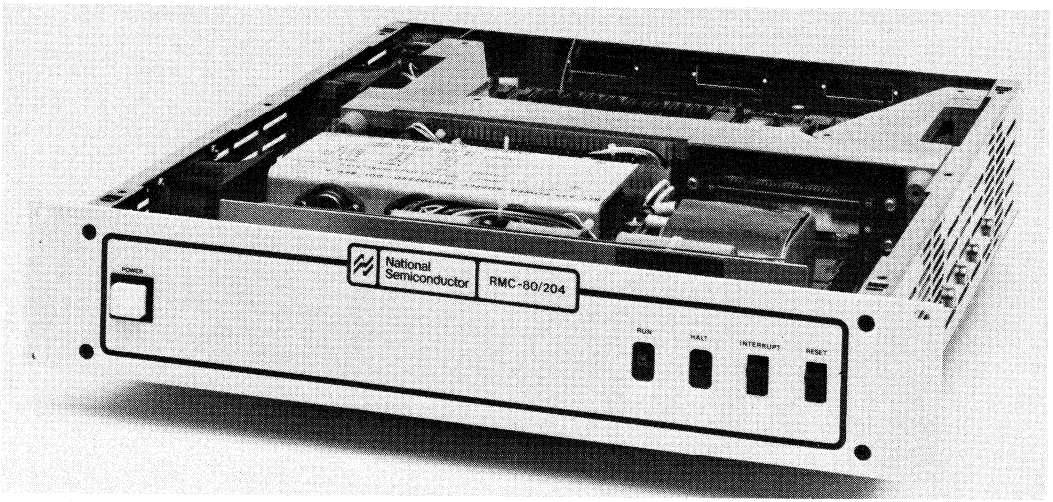
RMC-80/14	Rack Mountable Computer System, 110-115 VAC, 60 Hz
RMC-80/14E	Rack Mountable Computer System, 200-230 VAC, 50 Hz
	Both systems include: BLC-80/14 CPU board, BLC-635 Power Supply, BLC-604 Card Cage, BLC-910 System Monitor, a 115 volt power cable, 115 volt and 230 volt fuses, dual fans, 3 expansion slots, operator panel and documentation.

Documentation

420305620-001	RMC-80/14 Enclosure Monitor User's Manual
420305618-001	BLC-80P14 Prototyping Package User's Manual
420305489-001	BLC-635 Power Supply User's Manual

National Semiconductor

RMC-80/204
Rack Mountable Computer



- **Fully Self-Contained Rack Mountable Package for OEM Applications**
  - BLC-80/204 Board Level Computer
  - BLC-920 System Monitor for loading, executing, debugging programs
  - BLC-635 Power Supply
  - BLC-604 4-Slot Card Cage
- **Front Panel with Power, Reset, and Interrupt Switches and Halt and Run Status Indicators**
- **Rear Panel with Provision for User Installed Connectors**
- **Expandable with Standard BLC/SBC Series/80 Products**
- **Replacement for Intel's System 80/20 and System 80/20-4**

Product Overview

The RMC-80/204 is a packaged OEM microcomputer system based on the BLC-80/204 Board Level Computer. The RMC-80/204 occupies only 3½ inches of vertical space in a standard RETMA rack. The self-contained power supply has enough capacity to handle the BLC-80/204 CPU board plus three additional expansion boards. The chassis contains the CPU board, power supply, dual fans, and three expansion slots.

The RMC-80/204 may be expanded beyond the basic system through additional CPU boards, RAM and ROM expansion boards in any combination up to 64K bytes, various I/O controllers, digital and analog I/O, and other system modules.

Functional Description

BLC-80/204 CPU

The BLC-80/204 is a self-contained board level computer including the central processor, system clock, RAM and PROM memories, 48 I/O lines, an RS232C serial communications interface, hardware vectored interrupt logic, multiprocessor bus arbitration capability, three programmable timers, and bus logic and drivers.

The INS8080A-2 n-channel LSI microprocessor is the central processor for the BLC-80/204. The INS8080A-2 provides six general purpose 8-bit registers, an 8-bit accumulator, a 16-bit program counter and a 16-bit stack pointer register. The general purpose registers can be utilized singly or in pairs when double precision operations are required. The 16-bit program counter allows direct

addressing of a full 64K bytes of memory. The stack pointer controls addressing of an external stack located anywhere within the 64K memory space. The stack may be used to store the contents of the various registers while interrupts and subroutines are being services.

4K bytes of static read/write memory are provided by MM5257 RAM's while sockets for MM2708/MM2716 EPROM's or MM2308/MM2316E ROM's provide up to 8K bytes of read only memory in 1K or 2K increments. All ROM and RAM operations on the CPU board are performed at maximum processor speed.

BLC-604 Card Cage

A BLC-604 Card Cage accommodates the BLC-80/204 and up to three additional Series/80 boards. The backplane connects system bus signals and power to the board edge connector sockets and is cabled to the power supply.

BLC-635 Power Supply

The self-contained BLC-635 Power Supply is designed to power the CPU board and three additional expansion boards. Overvoltage and overcurrent protection is provided, and an AC Low signal is generated under low line conditions.

BLC-920 System Monitor Firmware

The system monitor is supplied with the RMC-80/204 in two preprogrammed MM2708 PROM's. This comprehensive monitor includes facilities to load, execute and debug programs. The monitor allows the user to examine and modify any RAM memory location or CPU register.

The system monitor also permits the insertion of breakpoints to facilitate software and hardware debugging and contains the following commands:

I	Insert into memory
X	Examine and modify CPU register
S	Substitute memory
M	Move memory
D	Display memory contents and addresses
A	Display memory contents in hex and ASCII
F	Display memory contents for search value
H	Display sum and difference
O	Write output byte
W	Write hexadecimal file
R	Read hexadecimal file
T	Display input port contents
G	Go execute program
N	Single step (next instruction)

Specifications

Refer to specifications for BLC-80/204, BLC-604, and BLC-635.

Front Panel

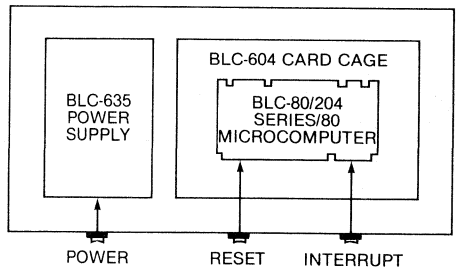
Switches —	Power On/Off Reset Interrupt		
Indicators —	Halt Run		
System Monitor —	Addresses	$0000-069C_{16}$ (ROM) $3F80-3FFF_{16}$ (RAM)	
Input Power —	100, 115, 215, 230 VAC ± 10% 47-63 Hz		
DC Power Available for Expansion Boards —	+12V, 1.65A +5V, 9.1A −5V, 0.7A −12V, 0.8A Assumes fully loaded CPU board with PROM's and terminators installed.		
Environmental —	Temperature 0° to 55°C Humidity 0 to 90% non-condensing		
Physical —	Height	3.5 in.	(8.89 cm)
	Width	19 in.	(48.26 cm)
	Depth	20 in.	(50.8 cm)
	Weight	37 lb.	(16.8 kg)

Order Information

RMC-80/204	Rack Mountable Computer System, 110-115 VAC, 60 Hz
RMC-80/204E	Rack Mountable Computer System, 200-230 VAC, 50 Hz
	Both systems include: BLC-80/204 CPU board, BLC-635 Power Supply, BLC-604 Card Cage, BLC-920 System Monitor, a 115 volt power cable, 115 volt and 230 volt fuses, dual fans, 3 expansion slots, operator panel and documentation.

Documentation

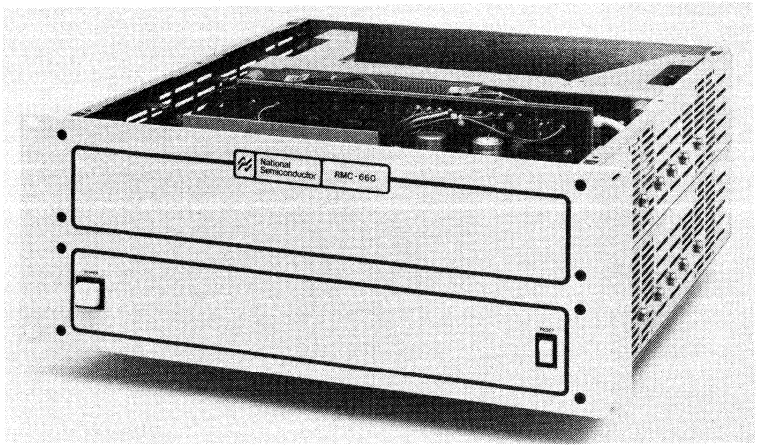
420305761-001	RMC-80/204 Enclosure Monitor User's Manual
420305883-001	RMC-80/204 System Package (3 manual set)
420305745-001	BLC-80P204 Prototyping Package User's Manual
420305489-001	BLC-635 Power Supply User's Manual



RMC-80/204 Diagram

National Semiconductor

RMC-660
System Chassis



- **Allows Large OEM Configuration of Series/80 Products**
  - 8-slot card cage
  - Heavy duty 30 Amp power supply
- **Front Panel with Power and Reset Switches for Control**
- **Rear Panel Accepts a Variety of User Connectors**
- **Plug-replacement for SBC-660 System Chassis**

Product Overview

The RMC-660 System Chassis supports Series/80 Board Level Computers and the full complement of expansion boards. The chassis occupies 7 inches of vertical rack space in a standard 19-inch RETMA rack. The System Chassis includes a BLC-665 Heavy Duty Power Supply, cooling fans, and an 8-slot card cage including a printed circuit board bus.

Functional Description

The BLC-665 Heavy Duty Power Supply provides regulated DC outputs of ±5 and ±12 volts. Current limiting and overvoltage protection is provided on all outputs. Logic provided in the power supply senses an AC power failure or low line condition and generates a TTL compatible signal for an orderly system shutdown sequence. The power supply is connected to the 8-slot card cage by a mating cable set.

The front panel contains a power on-off switch and a reset switch which connects to the system bus of a CPU for external system control.

The RMC-660 is ideal for OEM applications requiring up to 8 boards.

Specifications

Refer to detailed specifications for BLC-665 Heavy Duty Power Supply.

Front Panel Switches —	Power On/Off Reset		
Input Power —	100, 115, 215, 230 VAC ± 10% 47-63 Hz		
Environmental —	Temperature 0° to 55°C Humidity 0 to 90% non-condensing		
Physical —	Height	7.00 in.	(17.8 cm)
	Width	19.00 in.	(48.3 cm)
	Depth	20.00 in.	(50.8 cm)
	Weight	49 lb.	(22.2 kg)

Order Information

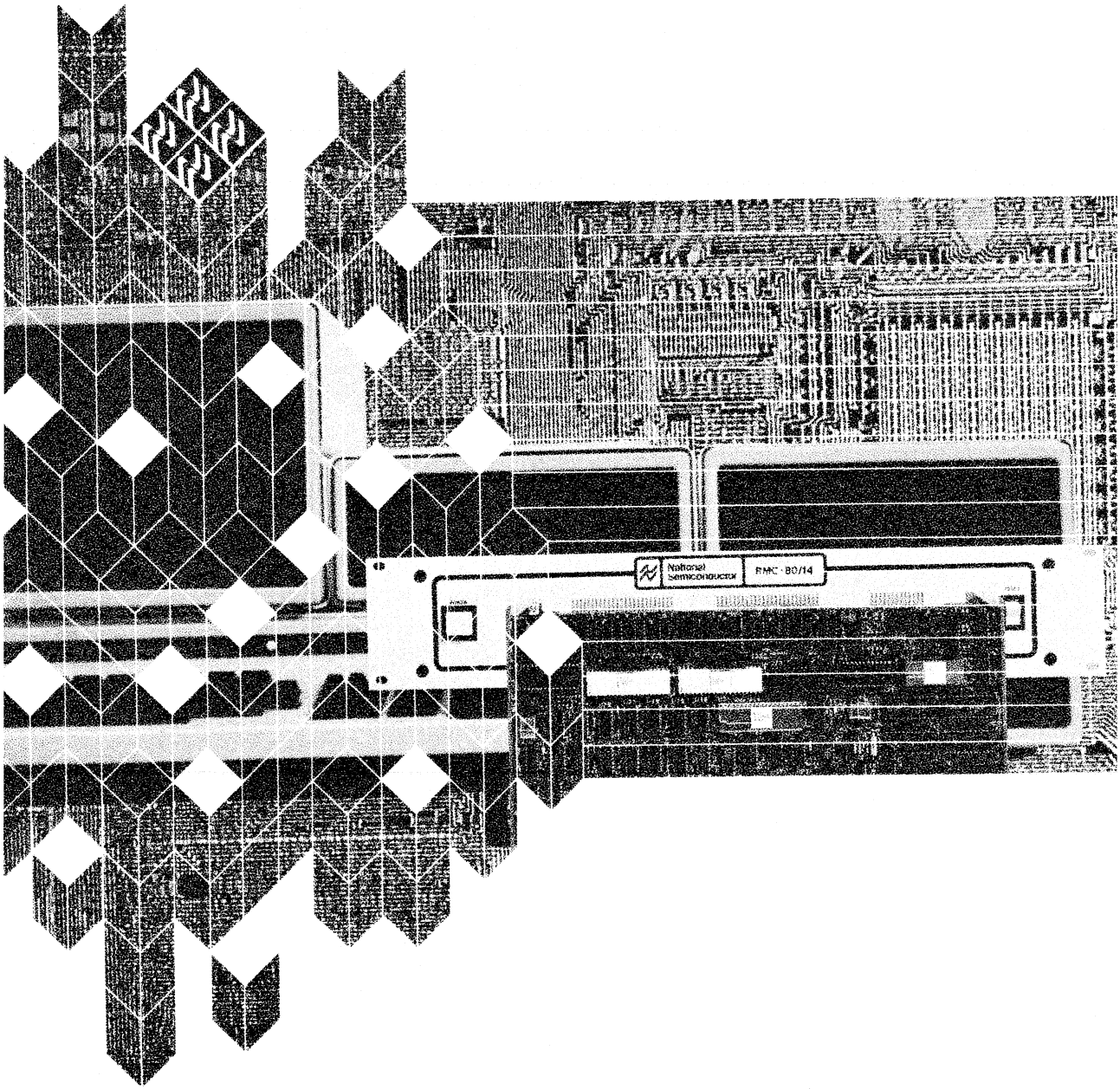
RMC-660	System Chassis, 110-115 VAC, 60 Hz.
RMC-660E	System Chassis, 200-230 VAC, 50 Hz.

Both systems include: card cage and backplane assembly, BLC-665 Heavy Duty Power Supply, 115 volt power cable, 115 volt and 230 volt fuses, 8-slot card cage, dual fans, backplane schematic drawing, RMC-660 assembly drawings and documentation.

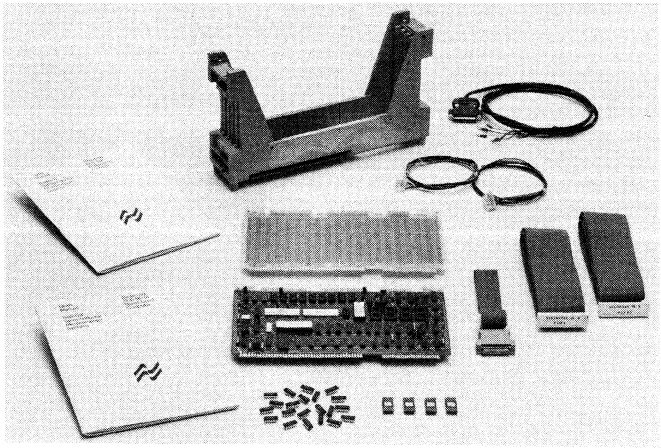
Documentation

420305561-001	RMC-660 Enclosure User's Manual
420302220-001	BLC-665 Power Supply User's Manual

Section 3
Prototyping Systems



BLC-80P
Prototyping Package



- **Basic Hardware for Fast Easy Prototyping**
  - BLC-80/10 CPU
  - Universal Prototyping Board
  - Card Cage
  - EPROM
- **Monitor Firmware**
  - Permits serial I/O communications
  - Eases system debugging task
  - Provides breakpoint capability
- **Accessories Allow Configuration Flexibility**
  - Terminators
  - Drivers
  - Cables

Product Overview

The BLC-80P Prototyping Package provides a convenient inexpensive method for OEM's to evaluate and design prototype Series/80 systems. Included are the BLC-80/10 CPU board with a BLC-910 monitor program in two PROM's. The monitor program permits loading, checking and modifying programs and data. In addition, the monitor program allows the user to set software and hardware breakpoints for system debugging.

A BLC-8905 Universal Prototyping Board and a BLC-604 Card Cage are also part of the prototyping package. The prototyping board allows users to develop custom interface circuitry for the system, while the card cage provides a convenient means to house and interconnect the boards. The card cage has two spare slots for installation of other Series/80 boards.

The accessories package in the BLC-80P contains several other system design aids: resistor terminators and line drivers for I/O, cables to connect a 20 milliamp or RS232C type terminal, cables to connect a power supply, and two spare MM2708 EPROM's for user program storage. The BLC-80P is supplied with complete documentation: schematics, drawings and manuals.

A wide variety of Series/80 products is available to complement the prototyping package: memory modules ranging from 4K to 64K bytes, I/O expansion, analog I/O, 14 Amp and 30 Amp power supplies, and a variety of cable, terminator and extender board accessories.

Functional Description

BLC-80/10 CPU

The BLC-80/10 is a self-contained board level computer including the central processor, system clock, RAM and ROM memories, I/O lines, serial communications interface, and bus logic and drivers.

The INS8080A n-channel LSI microprocessor is the central processor for the BLC-80/10. The 8080A provides six general purpose 8-bit registers, an accumulator, a 16-bit program counter and a 16-bit stack pointer register. The general purpose registers can be utilized singly, or in pairs where double precision operations are required. The 16-bit program counter allows direct addressing of a full 64K bytes of memory. The stack pointer controls addressing of an external stack located anywhere within the read/write memory, which may be used to store the contents of the various registers while interrupts and subroutines are being serviced.

1K bytes of static read/write memory are provided by 8 MM2111 RAM's while sockets for MM2708 EPROM's provide up to 4K bytes of read only memory in 1K increments. All ROM and RAM operations are performed at maximum processor speed.

BLC-604 Card Cage

A BLC-604 Card Cage accommodates the BLC-80/10 and up to three additional Series/80 boards. The backplane connects system bus signals and power to the board edge connector sockets and permits easy connection of the power supply cables. The system may be expanded in increments of four slots by adding BLC-614 Expansion Card Cages.

BLC-8905 Universal Prototyping Board

The universal prototyping board allows the user to construct custom interface circuits. The BLC-8905 plugs directly into the BLC-604 Card Cage which provides power and system signals to the board. Up to 108 16-pin wire-wrap sockets or a mix of 14, 16, 18, 22, 24, 28 and 40-pin sockets may be used on the board. Two 50 contact edge connectors and one 26 contact edge connector are provided for connection to flat cables identical to the cables supplied for the CPU I/O connectors.

BLC-910 System Monitor Firmware

The system monitor is supplied with the kit in two preprogrammed MM2708 PROM's. This comprehensive monitor includes facilities to load, execute and debug programs. The monitor allows the user to examine and modify any RAM memory location or CPU register. Programs may be loaded from or saved on paper tape by using an appropriate teletypewriter device and selecting the teletypewriter jumper options on the CPU board.

The system monitor permits the insertion of breakpoints to facilitate software and hardware debugging and contains the following commands:

I — Insert into memory

X — Examine and modify CPU register

S — Substitute memory

M — Move memory

D — Display memory

W — Write hexadecimal file

R — Read hexadecimal file

B — Write BNPF file

G — Go execute program

Accessories

The BLC-80P10 Prototyping Package provides several accessories to aid the user in initial system setup:

- Two blank MM2708 EPROM's
- DM7437 open collector inverting line drivers
- Ten BLC-902 1K ohm terminating resistor networks
- Ten BLC-901 220/330 ohm terminating resistor networks
- Two power supply cables to connect ±5, ±12 volts to the BLC-604 Card Cage backplane (2 feet long)
- Two 50-conductor I/O ribbon cables to connect BLC-80/10 or BLC-8905 I/O to external circuits/devices (5 feet long)
- One RS232C cable for connecting an RS232C serial I/O device (2.25 feet long)
- One 20ma current loop cable (TTY cable) for interconnecting the BLC-80/10 serial I/O port and a teletypewriter, CRT or other 20ma current loop device (5 feet long)

Specifications

Refer to Specifications for BLC-80/10, BLC-8905 and BLC-604.

Power — +5V, 2.9A
−5V, 0.02A
+12V, 0.05A
−12V, 0.15A

Environmental — Temperature 0° to 55°C
Humidity 0 to 90%
non-condensing

Physical —

Height	8.5 in.	(21.59 cm)
Width	14.2 in.	(36.07 cm)
Depth	3.34 in.	(8.48 cm)
Weight	3.4 lbs.	(1.5 kg)

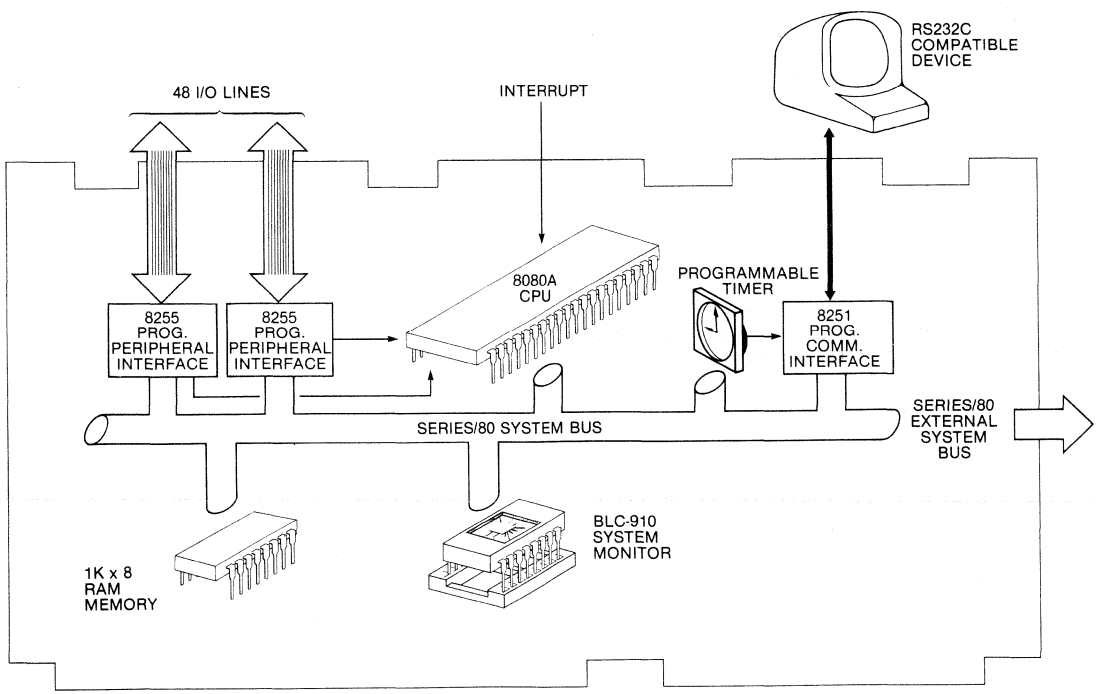
Order Information

BLC-80P Prototyping Package with a BLC-80/10 Board Level Computer including 1K bytes of static RAM and sockets for 2K bytes of EPROM. Includes monitor firmware, universal prototyping board, card cage, terminators, drivers and cables.

Documentation

420305521-001 BLC-80P Prototyping Package User's Manual.

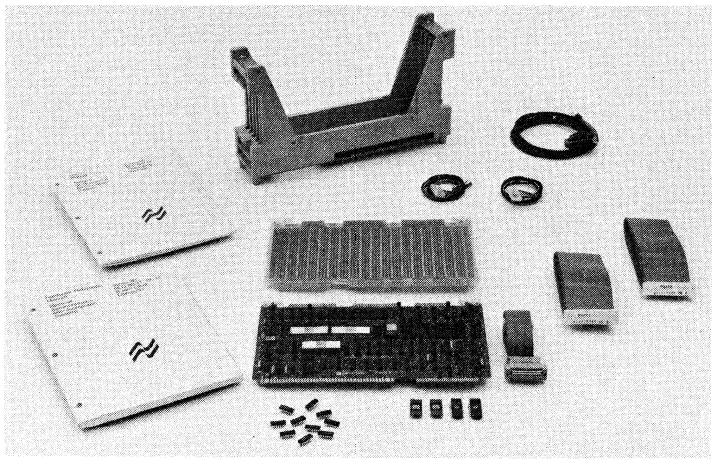
420305373-001 BLC-80/10 Board Level Computer Hardware Reference Manual.



BLC-80P Diagram

National Semiconductor

BLC-80P14
Prototyping Package



- **Basic Hardware for Fast Easy Prototyping**
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- **Monitor Firmware**
  - Permits serial I/O communications
  - Eases system debugging task
  - Provides breakpoint capability
- **Accessories Allow Configuration Flexibility**
  - Terminators
  - Drivers
  - Cables

Product Overview

The BLC-80P14 Prototyping Package provides a convenient inexpensive method for OEM's to evaluate and design prototype Series/80 systems. Included are the BLC-80/14 CPU board with a BLC-910 monitor program in two PROM's. The monitor program permits loading, checking and modifying programs and data. In addition, the monitor program allows the user to set software and hardware breakpoints for system debugging.

A BLC-8905 Universal Prototyping Board and a BLC-604 Card Cage are also part of the prototyping package. The prototyping board allows users to develop custom interface circuitry for the system, while the card cage provides a convenient means to house and interconnect the boards. The card cage has two spare slots for installation of other Series/80 boards.

The accessories package in the BLC-80P14 contains several other system design aids: resistor terminators and line drivers for I/O, cables to connect a 20 milliamp or RS232C type terminal, cables to connect a power supply, and two spare MM2708 EPROM's for user program storage. The BLC-80P14 is supplied with complete documentation: schematics, drawings and manuals.

A wide variety of Series/80 products is available to complement the prototyping package: memory modules ranging from 4K to 64K bytes, I/O expansion, analog I/O, 14 Amp and 30 Amp power supplies, and a variety of cable, terminator and extender board accessories.

Functional Description

BLC-80/14 CPU

The BLC-80/14 is a self-contained board level computer including the central processor, system clock, RAM and ROM memories, I/O lines, serial communications interface, and bus logic and drivers.

The INS8080A n-channel LSI microprocessor is the central processor for the BLC-80/14. The 8080A provides six general purpose 8-bit registers, an accumulator, a 16-bit program counter and a 16-bit stack pointer register. The general purpose registers can be utilized singly, or in pairs where double precision operations are required. The 16-bit program counter allows direct addressing of a full 64K bytes of memory. The stack pointer controls addressing of an external stack located anywhere within the read/write memory. The stack may be used to store the contents of the various registers while interrupts and subroutines are being serviced.

4K bytes of static read/write memory are provided by MM2114 RAM's while sockets for MM2708/MM2716 EPROM's or MM2308/MM2316E ROM's provide up to 8K bytes of read only memory in 1K or 2K increments. All ROM and RAM operations are performed at maximum processor speed.

BLC-604 Card Cage

A BLC-604 Card Cage accommodates the BLC-80/14 and up to three additional Series/80 boards. The backplane connects system bus signals and power to the board edge connector sockets and permits easy connection of the power supply cables. The system may be expanded in increments of four slots by adding BLC-614 Expansion Card Cages.

BLC-8905 Universal Prototyping Board

The universal prototyping board allows the user to construct custom interface circuits. The BLC-8905 plugs directly into the BLC-604 Card Cage which provides power and system signals to the board. Up to 108 16-pin wire-wrap sockets or a mix of 14, 16, 18, 22, 24, 28 and 40-pin sockets may be used on the board. Two 50 contact edge connectors and one 26 contact edge connector are provided for connection to flat cables identical to the cables supplied for the CPU I/O connectors.

BLC-910 System Monitor Firmware

The system monitor is supplied with the kit in two preprogrammed MM2708 PROM's. This comprehensive monitor includes facilities to load, execute and debug programs. The monitor allows the user to examine and modify any RAM memory location or CPU register. Programs may be loaded from or saved on paper tape by using an appropriate teletypewriter device and selecting the teletypewriter jumper options on the CPU board.

The system monitor permits the insertion of breakpoints to facilitate software and hardware debugging and contains the following commands:

I — Insert into memory

X — Examine and modify CPU register

S — Substitute memory

M — Move memory

D — Display memory

W — Write hexadecimal file

R — Read hexadecimal file

B — Write BNPF file

G — Go execute program

Accessories

The BLC-80P14 Prototyping Package provides several accessories to aid the user in initial system setup:

- Two blank MM2708 EPROM's
- Ten DM7437 open collector inverting line drivers
- Ten BLC-902 1K ohm terminating resistor networks
- Ten BLC-901 220/330 ohm terminating resistor networks
- Two power supply cables to connect ±5, ±12 volts to the BLC-604 Card Cage backplane (2 feet long)
- Two 50-conductor I/O ribbon cables to connect BLC-80/14 or BLC-8905 I/O to external circuits/devices (5 feet long)
- One RS232C cable for connecting an RS232C serial I/O device (2.25 feet long)
- One 20ma current loop cable (TTY cable) for interconnecting the BLC-80/14 serial I/O port and a teletypewriter, CRT or other 20ma current loop device (5 feet long)

Specifications

Refer to Specifications for BLC-80/14, BLC-8905 and BLC-604.

Power — +5V, 2.9A
−5V, 0.02A
+12V, 0.05A
−12V, 0.15A

Environmental — Temperature 0° to 55°C
Humidity 0 to 90%
non-condensing

Physical —

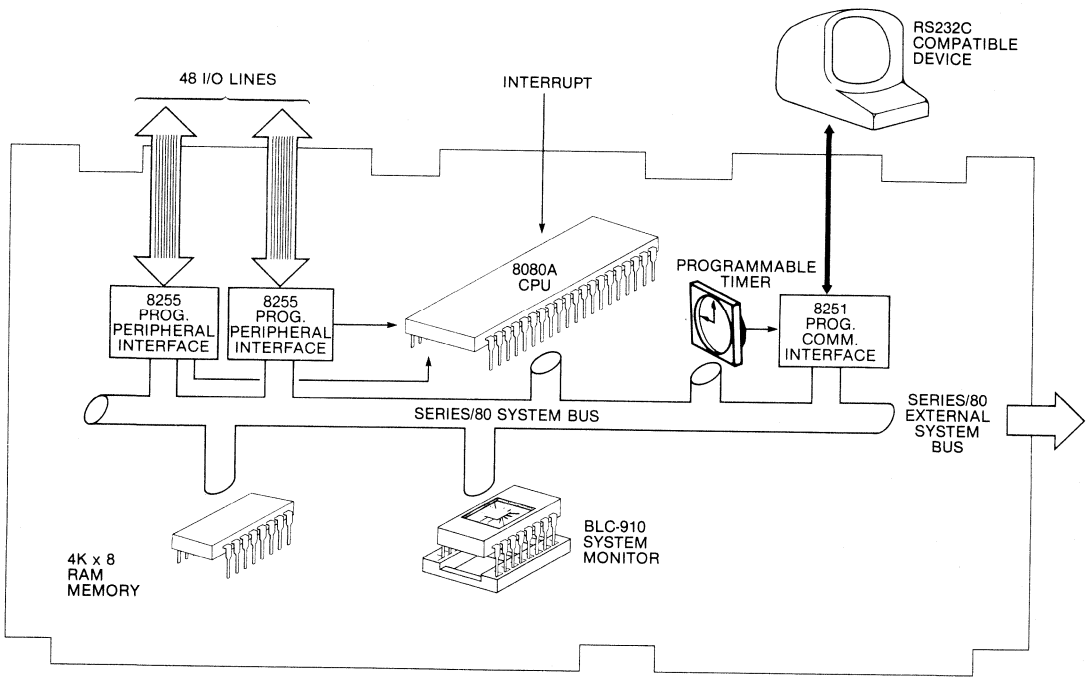
Height	8.5 in.	(21.59 cm)
Width	14.2 in.	(36.07 cm)
Depth	3.34 in.	(8.48 cm)
Weight	3.4 lbs.	(1.5 kg)

Order Information

BLC-80P14	Prototyping Package with a BLC-80/14 Board Level Computer including 4K bytes of static RAM and sockets for up to 8K bytes of EPROM. Includes monitor firmware, universal prototyping board, card cage, terminators, drivers and cables.

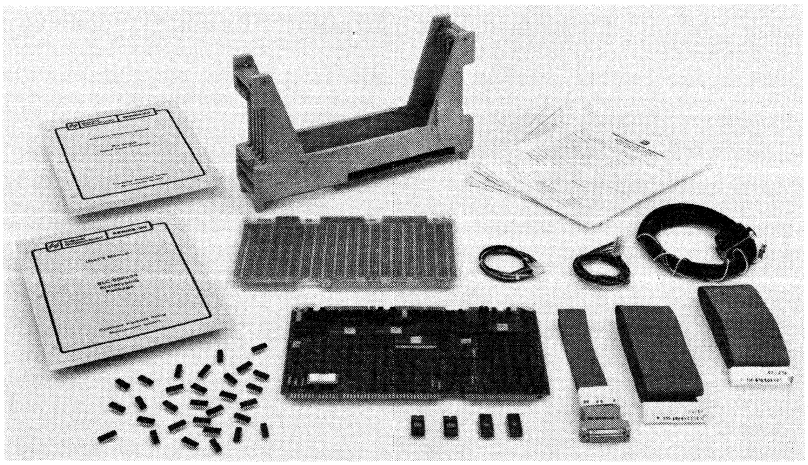
Documentation

420305618-001	BLC-80P14 Prototyping Package User's Manual.
420305532-001	BLC-80/11, 80/12, 80/14 Board Level Computer Hardware Reference Manual.



BLC-80P14 Diagram

BLC-80P204
Prototyping Package



- **Basic Hardware for Fast Easy Prototyping**
  - BLC-80/204 CPU
  - Universal Prototyping Board
  - Card Cage
  - EPROM
- **Monitor Firmware**
  - Permits serial I/O communications
  - Eases system debugging task
  - Provides breakpoint capability
- **Accessories Allow Configuration Flexibility**
  - Terminators
  - Drivers
  - Cables
  - Current Loop Adapter

Product Overview

The BLC-80P204 Prototyping Package provides a convenient inexpensive method for OEM's to evaluate and design prototype Series/80 systems. Included are the BLC-80/204 CPU board with a BLC-920 monitor program in two PROM's. The monitor program permits loading, checking and modifying programs and data. In addition, the monitor program allows the user to set software and hardware breakpoints for system debugging.

A BLC-8905 Universal Prototyping Board and a BLC-604 Card Cage are also part of the prototyping package. The prototyping board allows users to develop custom interface circuitry for the system, while the card cage provides a convenient means to house and interconnect the boards. The card cage has two spare slots for installation of other Series/80 boards.

The accessories package in the BLC-80P204 contains several other system design aids: resistor terminators and line drivers for I/O, cables to connect a 20 milliamp or RS232C type terminal, cables to connect a power supply, and two spare MM2708 EPROM's for user program storage. The BLC-80P204 is supplied with complete documentation: schematics, drawings and manuals.

A wide variety of Series/80 products is available to complement the prototyping package: memory modules ranging from 4K to 64K bytes, I/O expansion, analog I/O, 14 Amp and 30 Amp power supplies, and a variety of cable, terminator and extender board accessories.

Functional Description

BLC-80/204 CPU

The BLC-80/204 is a self-contained board level computer including the central processor, system clock, RAM and ROM memories, 48 I/O lines, an RS232C serial communications interface, hardware vectored interrupt logic, multiprocessor bus arbitration capability, three programmable timers, and bus logic and drivers.

The INS8080A-2 n-channel LSI microprocessor is the central processor for the BLC-80/204. The 8080A-2 provides six general purpose 8-bit registers, an accumulator, a 16-bit program counter and a 16-bit stack pointer register. The general purpose registers can be utilized singly or in pairs where double precision operations are required. The 16-bit program counter allows direct addressing of a full 64K bytes of memory. The stack pointer controls addressing of an external stack located anywhere within the read/write memory. The stack may be used to store the contents of the various registers while interrupts and subroutines are being serviced.

4K bytes of static read/write memory are provided by MM5257 RAM's while sockets for MM2708/MM2716 EPROM's or MM2308/MM2316E ROM's provide up to 8K bytes of read only memory in 1K or 2K increments. All ROM and RAM operations are performed at maximum processor speed.

BLC-604 Card Cage

A BLC-604 Card Cage accommodates the BLC-80/204 and up to three additional Series/80 boards. The backplane connects system bus signals and power to the board edge connector sockets and permits easy connection of the power supply cables. The system may be expanded in increments of four slots by adding BLC-614 Expansion Card Cages.

BLC-8905 Universal Prototyping Board

The universal prototyping board allows the user to construct custom interface circuits. The BLC-8905 plugs directly into the BLC-604 Card Cage which provides power and system signals to the board. Up to 108 16-pin wire-wrap sockets or a mix of 14, 16, 18, 22, 24, 28 and 40-pin sockets may be used on the board. Two 50 contact edge connectors and one 26 contact edge connector are provided for connection to flat cables identical to the cables supplied for the CPU I/O connectors.

BLC-920 System Monitor Firmware

The system monitor is supplied with the kit in two preprogrammed MM2708 PROM's. This comprehensive monitor includes facilities to load, execute and debug programs. The monitor allows the user to examine and modify any RAM memory location or CPU register.

The system monitor permits the insertion of breakpoints to facilitate software and hardware debugging and contains the following commands:

I — Insert into memory

X — Examine and modify CPU register

S — Substitute memory

M — Move memory

D — Display memory contents and address

A — Display memory contents

F — Display memory contents for search value

H — Display sum and difference

O — Write output byte

W — Write hexadecimal file

R — Read hexadecimal file

T — Display input port contents

G — Go execute program

N — Single step (next instruction)

Accessories

The BLC-80P204 Prototyping Package provides several accessories to aid the user in initial system setup:

- Two blank MM2708 EPROM's
- Ten DM7437 open collector inverting line drivers
- Ten BLC-902 1K ohm terminating resistor networks
- Ten BLC-901 220/330 ohm terminating resistor networks
- Two power supply cables to connect ±5, ±12 volts to the BLC-604 Card Cage backplane (2 feet long)
- Two 50-conductor I/O ribbon cables to connect BLC-80/204 or BLC-8905 I/O to external circuits/devices (5 feet long)
- One RS232C cable for connecting an RS232C serial I/O device (2.25 feet long)
- One 20ma current loop cable (TTY cable) for interconnecting the BLC-80/204 serial I/O port and a teletypewriter, CRT or other 20ma current loop device (5 feet long)
- One BLC-530 Current Loop Adapter

Specifications

Refer to Specifications for BLC-80/204, BLC-8905 and BLC-604.

Power — +5V, 4.9A
−5V, 0.18A
+12V, 0.35A
−12V, 0.02A

Environmental — Temperature 0° to 55°C
Humidity 0 to 90%, non-condensing

Physical —			
	Height	8.5 in.	(21.59 cm)
	Width	14.2 in.	(36.07 cm)
	Depth	3.34 in.	(8.48 cm)
	Weight	4 lbs.	(1.8 kg)

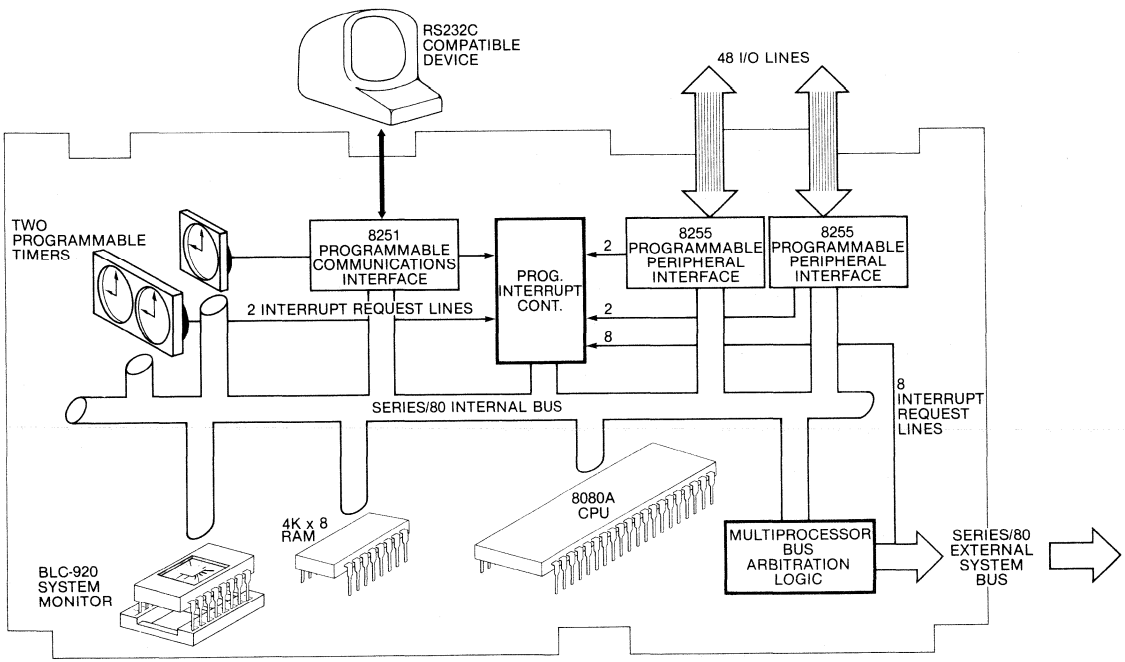
Order Information

BLC-80P204 Prototyping Package with a BLC-80/204 Board Level Computer including 4K bytes of static RAM and sockets for 4K bytes of EPROM using MM2708 modules or 8K bytes of EPROM using MM2716 modules. Includes monitor firmware, universal prototyping board, card cage, terminators, drivers, cables, and current loop adapter.

Documentation

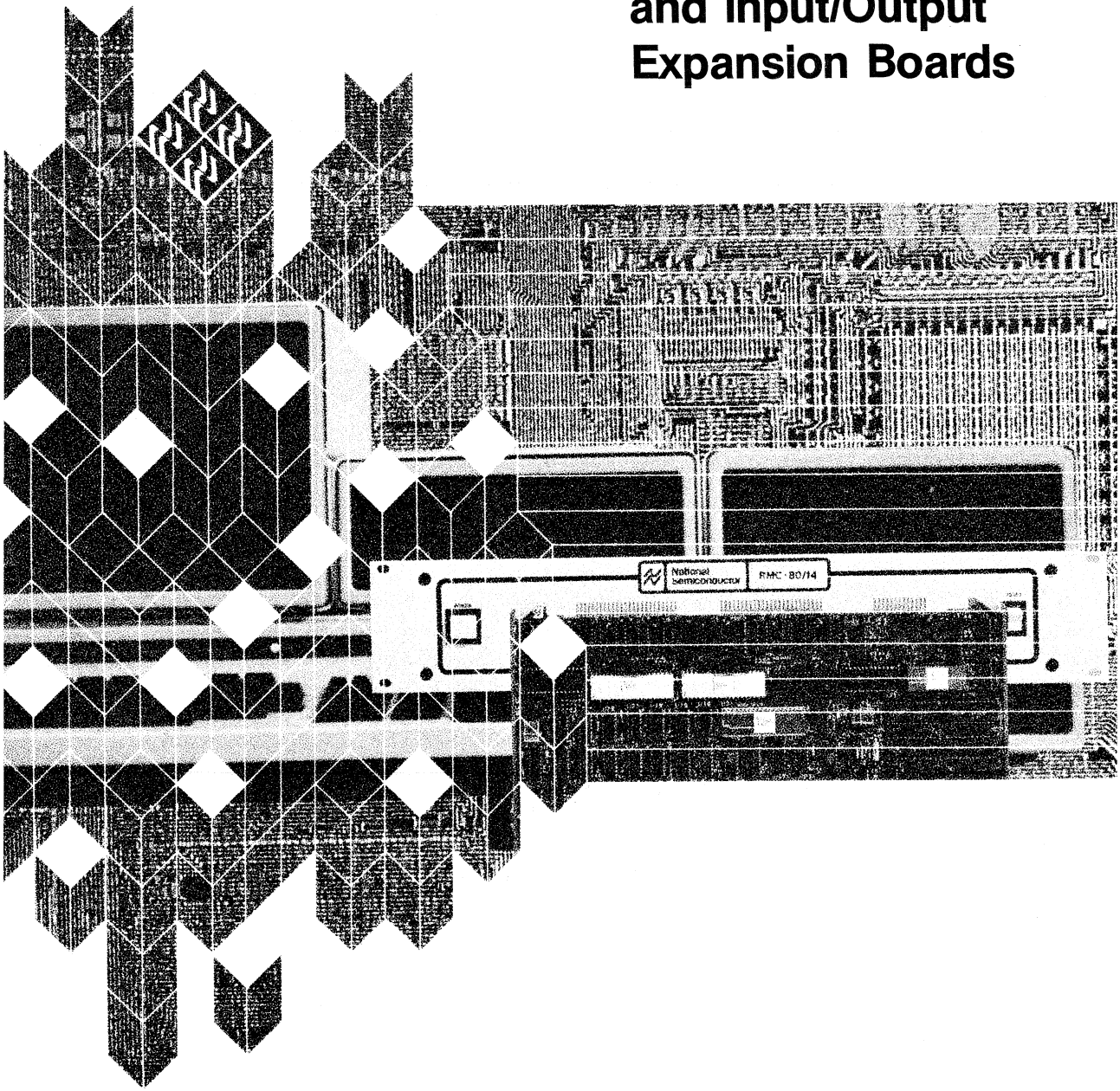
420305745-001 BLC-80P204 Prototyping Package User's Manual.

420305521-001 BLC-80/204 Board Level Computer Hardware Reference Manual.



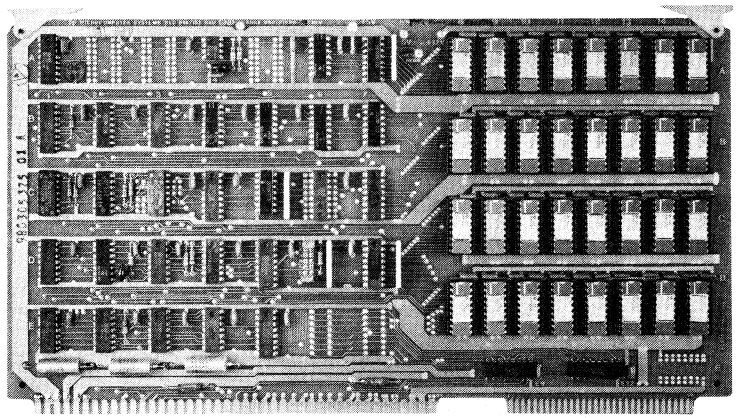
BLC-80P204 Diagram

Section 4
Memory and Combination Memory and Input/Output Expansion Boards



National Semiconductor

BLC-016
RAM Memory Board



- **Flexible System Implementation**
  - User-selectable starting address
  - 16K to 64K bytes in a single Series/80 system
- **On-board Refresh Eliminates the Need for a Separate Control Board**
- **Ease of Maintenance**
  - Socketed MM5271 4K x 1 dynamic RAM's
  - Address selection using BERG™ jumpers
- **Fully Compatible with BLC/SBC Products**
  - Plug-replacement for Intel's SBC-016

Product Overview

The BLC-016 is a member of a family of Series/80 memory and I/O expansion boards available from National Semiconductor. Compatible with all National Series/80 CPU boards, the BLC-016 plugs directly into any Series/80 card cage or system.

Flexible design allows selection of memory starting addresses to suit the system configuration. This is especially important when using a mix of memory increments or memory board capacities.

Functional Description

Based on National's MM5271 dynamic 4K x 1 RAM, the BLC-016 includes read/write data buffers, TTL compatible data, address and command lines, and on-board refresh logic.

On-board refresh of the entire 16K bytes of RAM is accomplished every two milliseconds. Each refresh cycle takes 700 nanoseconds, with a 64-bit block in each of the 32 MM5271 dynamic RAM's refreshed every 29 microseconds. System stability is maintained by inhibiting refresh when a read or write cycle is in progress.

High impedance TRI-STATE™ buffers are employed where address, data and command functions interface with the Series/80 system bus.

Address selection is implemented in contiguous 16K byte blocks beginning at memory locations 0000_{16}, 4000_{16}, 8000_{16}, or $C000_{16}$. Memory addresses used by the CPU on-board RAM and ROM are not available to the BLC-016 except for CPU's containing on-board RAM/ROM disable capability. Address blocks are easily selected using BERG™ jumper plugs.

Up to four BLC-016 RAM boards or a total of 64K bytes may be used in a single Series/80 system.

The array of 32 MM5271 RAM's is socketed for ease of troubleshooting, repair and maintenance of the BLC-016 board. Spare components may be inventoried rather than entire boards.

Specifications

Memory Size —	16K bytes
Word Size —	8 bits
Cycle Times —	Read — 700 ns Write — 1160 ns Refresh — 700 ns
Address Selection —	Jumper selection of contiguous 16K byte blocks starting at locations 0000_{16}, 4000_{16}, 8000_{16}, or $C000_{16}$
System Bus Interface —	Data, address and command signals are TRI-STATE™ TTL compatible
System Bus Connector —	86 contact double-sided card cage edge connector on 0.156 inch centers
Power —	+5V, 1.5A −5V, 0.01A +12V, 0.7A
Environmental —	Temperature 0° to 55°C Humidity 0 to 90% non-condensing

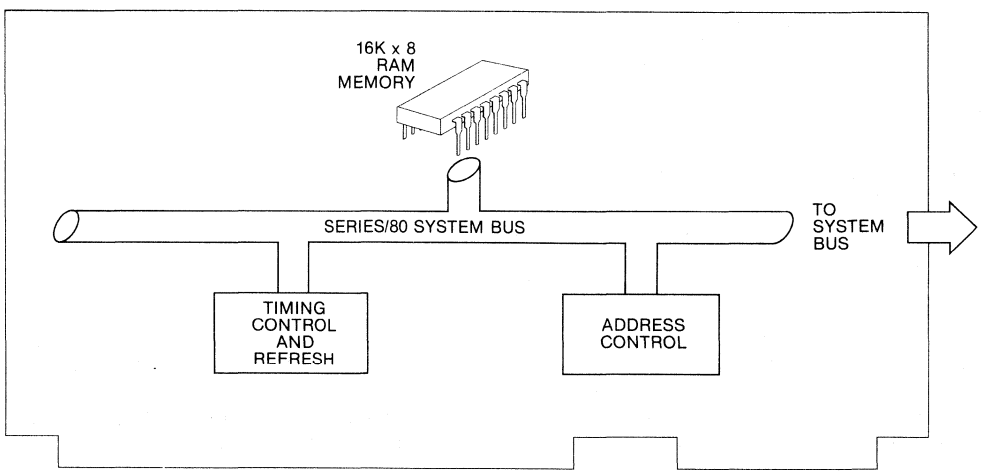
Physical —			
	Height	6.75 in.	(17.15 cm)
	Width	12.00 in.	(30.48 cm)
	Depth	0.50 in.	(1.27 cm)
	Weight	12 oz.	(340.2 g)

Order Information

BLC-016	16K Byte RAM Board

Documentation

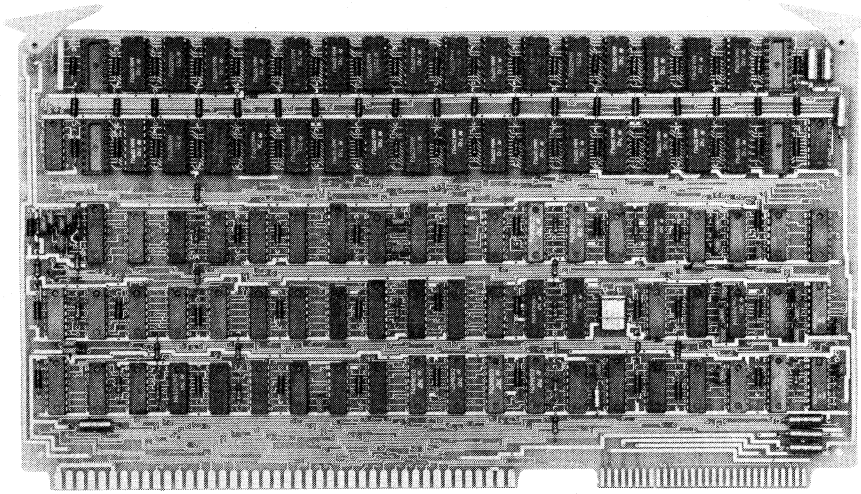
420305375-001	BLC-016 16K Byte RAM Board User's Manual.



BLC-016 Diagram

National Semiconductor

BLC-032, BLC-048, and BLC-064 RAM Memory Boards



- **Flexible System Configuration**
  - BLC-032 — 32K bytes
  - BLC-048 — 48K bytes
  - BLC-064 — 64K bytes
  - 8 or 16-bit data access
  - Optional byte parity
- **Enhance System Performance**
  - On-board refresh and control logic
  - Synchronized (transparent) refresh capability — no refresh wait state with BLC-80/204
  - Auxiliary power bus and memory protect logic for battery backup requirements
- **Ease of Maintenance**
  - Socketed MM5290 16K x 1 dynamic RAM's
- **Fully Compatible with BLC/SBC Products**
  - Plug-replacements for SBC-032/048/064

Product Overview

The BLC-032, BLC-048 and BLC-064 RAM expansion boards are designed to meet large memory requirements without sacrificing space or significantly reducing available power. These boards provide 32K bytes, 48K bytes and 64K bytes, respectively, of dynamic random access read/write memory (RAM) on a single printed circuit board. The boards are complete with all refresh and control electronics, address and data buffers, and memory array.

Designed-in flexibility permits the user to obtain the optimum system configuration. Starting address segments are provided at 16K byte boundaries and data may be accessed in 8- or 16-bit modes. Memory may be expanded up to one megabyte in a single Series/80 system by using the BLC-064 and implementing logic to activate additional existing address bits.

The BLC-032, BLC-048 and BLC-064 are plug-compatible replacements for Intel's SBC-032, 048 and 064 and plug directly into any BLC/SBC system.

Functional Description

The BLC-032, 048 and 064 are based on National's MM5290 16K x 1-bit dynamic RAM module. Memory access time is a fast 430 nanoseconds and a full read or write cycle takes only 660 nanoseconds. The memory complement is organized into independent 16K x 8-bit address blocks. Each block may be configured to a unique starting address on one of four 16K byte boundaries. In the case of the BLC-032 and BLC-048 this allows the user greater flexibility when using other Series/80 system ROM/PROM memory or I/O boards.

The board can be used in an eight or sixteen bit data mode. A separate control signal on the Series/80 system bus provides data mode selection under system control.

The BLC-032, 048 and 064 have a 20-bit address bus. This permits the sophisticated user to combine up to 16 BLC-064 RAM boards to create a megabyte memory system. Normally, 8080 based systems use only 16 of the 20 available address bits; however, board select logic may be enabled to allow a BLC-064 to occupy any one of sixteen 64K byte blocks within a megabyte address range.

Synchronized Refresh

On-board automatic refresh logic is used to refresh a portion of the total memory every 13 microseconds. Refresh logic waits for an in-process memory access cycle to be completed before initiating a refresh cycle. In addition, there is a special status signal implemented on the BLC-80/204 microcomputer for refresh synchronization. When enabled, this feature causes BLC-032, 048 and 064 memory refresh cycles to synchronize with CPU activity and results in increased system throughput and consistent software timing loop results.

Memory Protect

Memory protection of RAM contents is provided through an auxiliary connector on the memory board. The logic connected to this line is TTL compatible and, when asserted as an active low from an external source, disables read and write access functions. This input is provided for the protection of RAM contents during a system power-down sequence.

Specifications

Memory Size — BLC-032 — 32K bytes
BLC-048 — 48K bytes
BLC-064 — 64K bytes

Word Size — 8 or 16 bits

Access Time — 430 ns

Cycle Times — Read — 660 ns
Write — 660 ns (delayed write)
1230 ns (advanced write)
Refresh — 615 ns

Address Selection — Jumper selection of contiguous 16K byte blocks starting at locations 0000_{16}, 4000_{16}, 8000_{16}, or $C000_{16}$

Parity — Factory installed option — consult factory for details

System Bus Interface — Data, address and command signals are TRI-STATE™ TTL compatible

System Bus Connector — 86 contact double-sided card cage edge connector on 0.156 inch centers

Auxiliary Power — Separate power bus provided for systems requiring battery backup of memory for critical applications. On-board jumpers provided to enable this mode of operation.

Power —

	Operating	Battery
+5V	3.0 A	1.7 A
−5V	0.011 A	0.011 A
+12V	0.47 A	0.140 A

Environmental — Temperature 0° to 55 °C
Humidity 0 to 90% non-condensing

Physical —

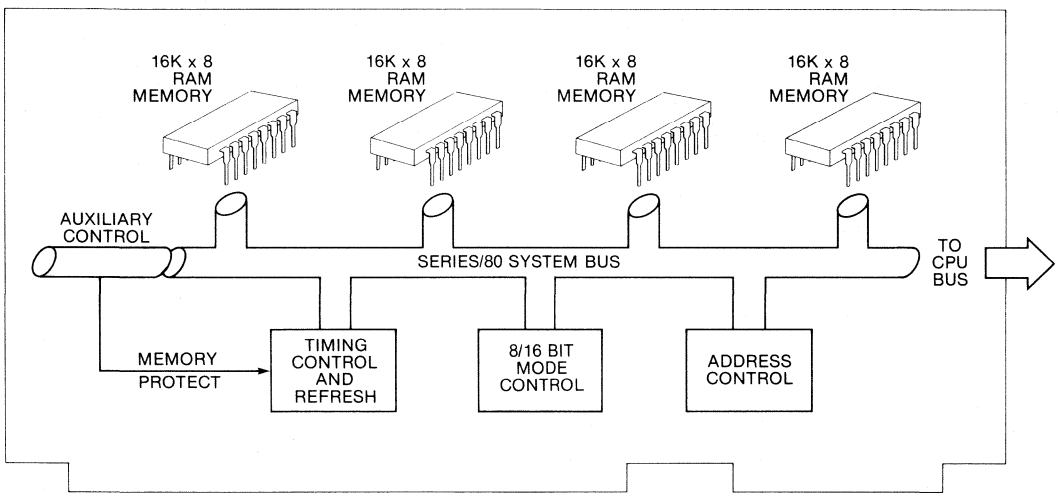
Height	6.75 in.	(17.15 cm)
Width	12.00 in.	(30.48 cm)
Depth	0.50 in.	(1.27 cm)
Weight	14 oz.	(396.9 g)

Order Information

BLC-032	32K Byte RAM Board
BLC-048	48K Byte RAM Board
BLC-064	64K Byte RAM Board

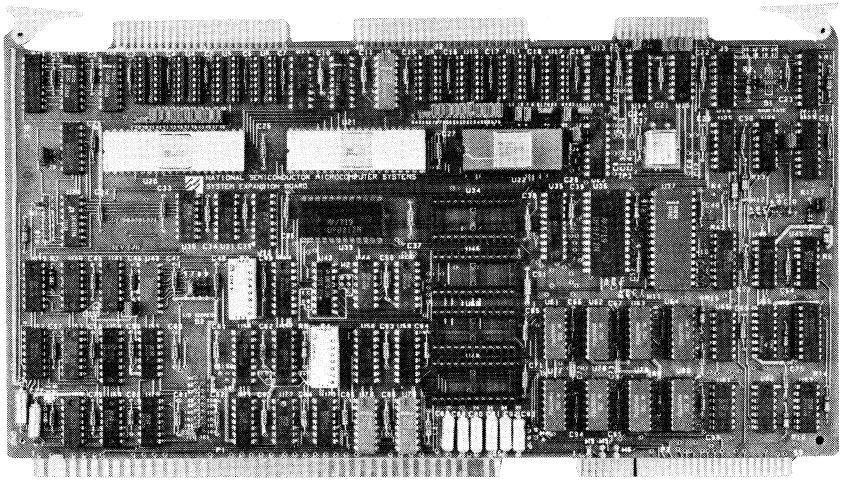
Documentation

420305529-001	BLC-032, 048, 064 32K, 48K, 64K Byte RAM Board Hardware Reference Manual.



BLC-064 Diagram

BLC-104 and BLC-116 Memory and Input/Output Boards



- **Flexible Memory Combinations**
  - 4K RAM and up to 8K PROM
  - 16K RAM and up to 8K PROM
  - 4K byte address boundaries
  - ROM can be implemented in 1K segments
- **Battery Back-Up Logic for System Memory Integrity**
- **48 Programmable Input/Output Lines for Digital Control Applications**
- **Synchronous/Asynchronous Serial Channel Permits Data Communication Interfacing to Data Set or Data Terminal with Baud Rates of 75 to 38.4K**
- **8 Maskable Interrupts and 1 millisecond Timer Permit Easy System Control**
- **Plug-replacements for SBC-104 and SBC-116**

Product Overview

The BLC-104 and BLC-116 Memory and Input/Output Expansion Boards provide a combination of memory and digital input/output capability ideally suited to smaller system applications where space and system optimization are critical.

Memory is provided for both read/write and read only requirements. The BLC-104 contains 4K bytes of dynamic RAM and sockets for up to 8K bytes of PROM while the BLC-116 contains 16K bytes of dynamic RAM and sockets for up to 8K bytes of PROM. ROM/PROM is implemented using MM2308/MM2316E ROM modules or MM2708/MM2716 PROM modules.

Both parallel and serial input/output are provided — 48 programmable parallel lines and one synchronous/asynchronous serial port. The 48 line programmable input/output capability may be configured to provide a variety of unidirectional and bidirectional combinations. The serial channel is capable of data transmission rates of up to 38.4K baud. Maskable interrupts and a one millisecond timer are included to provide complete system control.

The BLC-104 and BLC-116 are plug-replacements for Intel's SBC-104 and SBC-116 boards.

Functional Description

Read/Write Memory

The BLC-104 read/write RAM is based on National's MM4027 4K x 1-bit dynamic RAM modules; the BLC-116 uses MM4116 15K x 1-bit dynamic RAM modules. RAM modules are socket mounted for fast troubleshooting and repair. Memory access time is 575 nanoseconds and a full read or write cycle takes only 665 nanoseconds. Memory refresh is asynchronous and independent of the CPU. RAM addressing is switch selected, permitting its use on any 4K byte boundary within the 64K byte address range of the system.

Memory contents may be protected by using an auxiliary connector on the board. The logic connected to this line is TTL compatible and, when asserted as an active low from an external source, disables read and write access functions. This feature protects RAM contents during a system power-down sequence and permits the battery back-up to maintain the memory refresh function.

Read Only Memory

The ROM section is designed to accept MM2708/MM2716 Programmable Read Only Memory (PROM) or MM2308/MM2316E ROM modules. While four sockets are provided for the maximum configuration, only the number of PROM modules required for the application are necessary. ROM access time is a fast 465 nanoseconds with a maximum full cycle time of 685 nanoseconds.

The ROM section address is switch selected, permitting its use on any 4K byte boundary within the 64K byte address range of the system.

Parallel Input/Output

The 48 input/output lines are controlled by two INS8255 Programmable Peripheral Interface Circuits. Using standard Series/80 instructions, the 48 lines may be configured to a variety of 4 and 8 parallel line segments capable of latched or unlatched operation in bidirectional modes. The parallel input/output section is divided into six ports, each containing 8 bits.

Three basic modes of operation may be selected by program instructions:

- Data read or write to the specified port without the use of handshake signals. Output data is latched while input data is unlatched.
- Data read or write to the specified port using strobe or handshake signals created by or transmitted to the interfaced external device.
- Data read or write to the specified port using a bidirectional port to communicate with the external device. Handshake signals are provided by a separate "control" port (port 3 or 6).

Input/output modes for all ports are defined in Appendix B. Sixteen input/output lines have 8226 type bidirectional drivers and terminators permanently installed. The remaining 32 lines are fitted with sockets to permit user selection of drivers and terminators to match specific line characteristics. Line drivers and terminators circuits are contained in 14 pin DIP packages.

National's BLC-901 and BLC-902 terminator modules are available as options to satisfy termination requirements. The BLC-901 contains 220/330 ohm divider type circuits for four lines, while the BLC-902 contains 1K ohm pull-up type terminator circuits for four lines. Figure 1 illustrates the terminator circuit configuration.

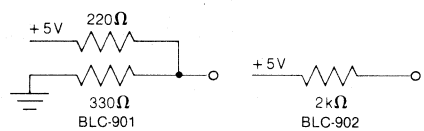


Figure 1. BLC-901 and BLC-902 Terminators

A variety of TTL compatible driver circuit types is available: inverting, non-inverting, high voltage and open collector combinations with sink current capacity ranging from 16 to 48 milliamps (see Table I).

Table I. Drivers

Type	Output	Current (ma)
7400	I	16
7403	I, OC	16
7408	NI	16
7409	NI, OC	16
7426	I, OC, HV	16
7432	NI	16
7437	I	48
7438	I, OC, HV	48

(I = inverting; NI = non-inverting; OC = open collector; HV = high voltage)

Serial Input/Output

The serial I/O port control is based on a Universal Synchronous/Asynchronous Receiver/Transmitter (USART) circuit. The port is fully EIA RS232C compatible, thereby allowing interface with a wide range of data sets and data terminals. Standard Series/80 instructions control data transmission, and software is used to implement the desired transmission protocol technique. The port is double buffered for full duplex transmissions and

contains full data set control to and from modems. Character framing and transmission mode parameters are controlled by programmable features and jumpers.

Synchronous transmission features:

- 5-, 6-, 7- or 8-bit characters
- Automatic SYNC character insertion, 1 or 2 characters
- SYNC search
- External synchronization
- Even or odd parity

Asynchronous transmission features:

- 5-, 6-, 7- or 8-bit characters
- Odd, even or no parity
- 1, 1½ or 2 stop bits
- False start bit detect
- Break character generation

Baud rate may be selected from the range 75 through 38.4K. Table II lists the rates available for synchronous and asynchronous data transmission. Three baud rates, based on a multiple of X1, X16 or X64 of the basic frequency, are program selectable.

Table II. Baud Rates

Synchronous	Asynchronous	
6980	75	1200
4800	110	2400
9600	150	4800
19200	300	9600
38400	600	19200

Error and status conditions are presented in the status word. Error condition may result from a framing error, data overrun (new character arrives before the buffer is empty) or incorrect parity. Figure 2 illustrates the status word.

The RS232C serial port may be converted to 20 ma current loop operation with an optionally available BLC-530 Current Loop Adapter. This permits interfacing devices such as teletypewriters, video displays and others not containing an RS232C compatible interface.

Interrupts

The BLC-104 and BLC-116 are designed to handle up to eight interrupt requests. Four may be jumper selected to permit automatic interrupt when a parallel character is received from or output to an external device.

Two interrupts may be configured to signal serial port character received and character transmitted.

The two remaining interrupt lines are shared by the 1 millisecond interval timer and two external event signal inputs.

The eight interrupts may be OR tied to form a single interrupt line to a system processor such as a BLC-80/10, or may be discrete when used with a system processor such as a BLC-80/204.

The eight interrupts may be individually masked under program control. The status of the interrupts is available to the system via the mask register.

I/O Section Addressing

The input/output section uses 16 contiguous addresses. The base, or board, address is jumper selectable to permit a high degree of system integration flexibility.

7	6	5	4	3	2	1	0
Data Set Ready	SYNC Detect	Framing Error	Data Overrun	Parity Error	Transmit Enable	Ready to Receive	Ready to Transmit

Figure 2. Status Word

Specifications

RAM Memory

Memory Size — BLC-104 — 4K bytes
BLC-116 — 16K bytes

Word Size — 8 bits

Access Time — 575 ns

Cycle Time — Read 665 ns
Write 665 ns
Refresh

Address Select — Switch and jumper selection
4K byte boundaries

ROM Memory

Memory Size — 4K bytes (ROM)
8K bytes (PROM)

Word Size — 8 bits

Access Time — 465 ns

Address Select — Switch and jumper selection
4K byte boundaries

Parallel Input/Output

Number of Ports — 6

Number of Lines — 48

Configuration — Single, 4- or 8-bit

Data Transfer Modes — Unidirectional and bidirectional

Data Control — Latched, unlatched and strobed

Interface — TTL compatible

Compatible I/O Driver Modules —

Type	Output	Current (ma)
7400	I	16
7403	I, OC	16
7408	NI	16
7409	NI, OC	16
7426	I, OC, HV	16
7432	NI	16
7437	I	48
7438	I, OC, HV	48

(I = inverting; NI = non-inverting;
OC = open collector;
HV = high voltage)

Compatible I/O Termination Modules — BLC-901 220/330 ohm divider
BLC-902 1K ohm pull-up

Serial Input/Output

Control — Programmable USART

Transmission Modes — Synchronous and asynchronous

Character Length — 5-, 6-, 7- or 8-bit

Parity — Odd, even or none

SYNC Functions — SYNC search
Automatic 1 or 2 SYNC character insertion

Asynchronous Stop Bits — 1, 1½ or 2

Asynchronous Break — Programmable control generation

Baud Rates — (asynchronous program controlled)

75	2400
110	4800
150	6980
300	9600
600	19200
1200	38400

External SYNC Control — Yes

Error Detection — Framing
Data overrun
Parity

Interface — RS232C

Interrupt — 8 lines
Program maskable
Discrete/OR tie capability

Timer — 1 millisecond intervals

System Bus Interface

All address, data and control signals are TRI-STATE™ TTL compatible.

Connectors

System Bus — 86 contact double-sided card cage edge connector on 0.156 inch centers

Auxiliary — 60 contact double-sided edge connector on 0.1-inch centers
Recommended mating connector:
3M "Schotchflex" 3463-001

Parallel I/O — 50 contact double-sided edge connector on 0.1-inch centers
Recommended mating connector:
3M 3415-001
AMP 2-86792-3
Recommended cables:
BLC-956 Parallel I/O Cable Kit
(two 5 foot ribbon cables)

Serial I/O	26 contact double-sided edge connector on 0.1-inch centers Recommended mating connector: 3M 3462-0001 flat AMP 1-583715-1 round

Power

	BLC-104	BLC-116	Battery
+5V	4.1 A	4.6 A	0.9 A
−5V	0.19 A	0.19 A	0.002 A
+12V	0.65 A	0.65 A	0.3 A
−12V	0.05 A	0.05 A	—

(Assumes ROM and I/O drivers installed.)

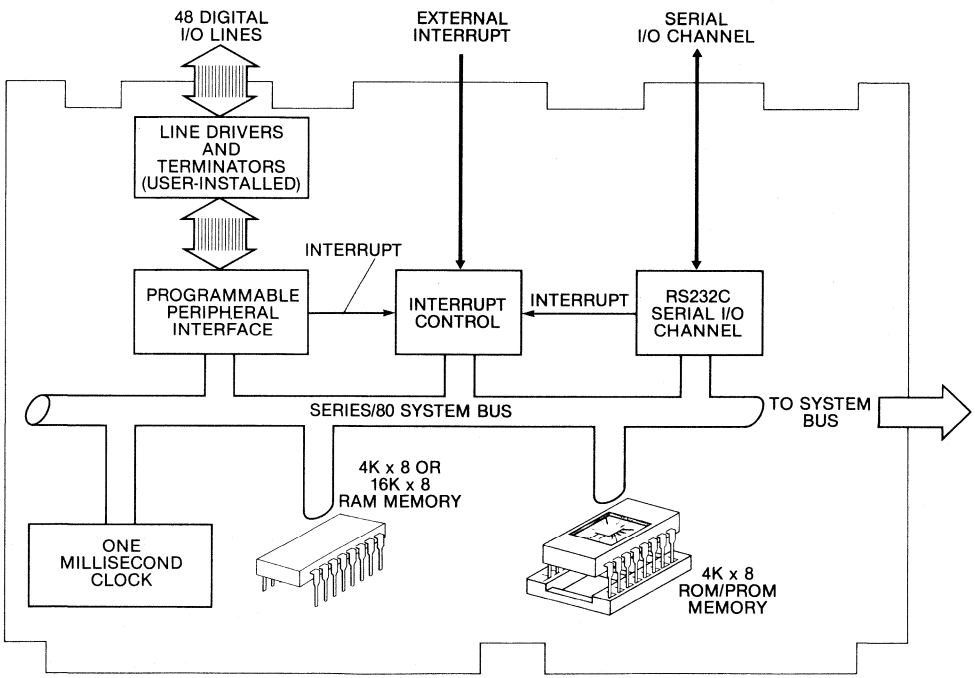
Environmental	Temperature 0° to 55°C Humidity 0 to 90% non-condensing		
Physical	Height	6.75 in.	(17.15 cm)
	Width	12.0 in.	(30.48 cm)
	Depth	0.50 in.	(1.27 cm)
	Weight	14 oz.	(396.9 g)

Order Information

BLC-104	RAM, ROM and I/O Expansion Board. Contains 4K bytes of dynamic RAM, sockets for 4K bytes of ROM or 8K bytes of PROM, 48 parallel and one serial I/O lines and 1 millisecond interval clock.
BLC-116	RAM, ROM and I/O Expansion Board. Contains 16K bytes of dynamic RAM, sockets for 4K bytes of ROM or 8K bytes of PROM, 48 parallel and one serial I/O lines, and a 1 millisecond interval clock.

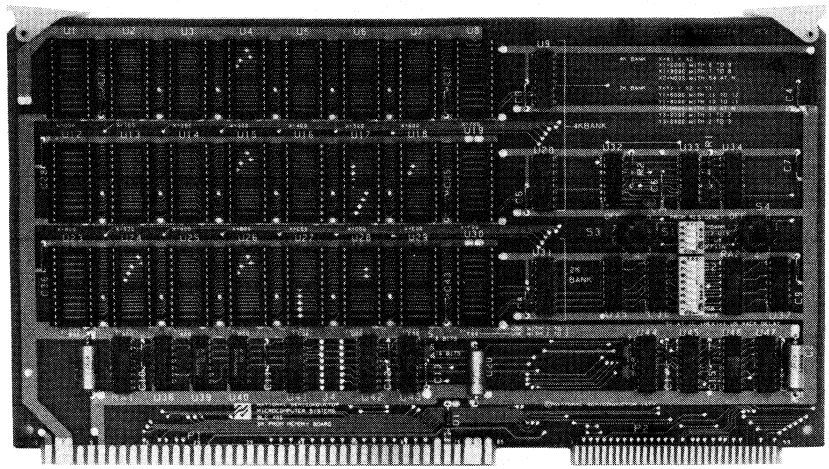
Documentation

420305376-001	BLC-104/116/517 Input/Output and Memory Expansion Boards Hardware Reference Manual.



BLC-104 and BLC-116 Diagram

BLC-406
6K Byte Read Only Memory Board



- **6K Bytes of Non-Volatile ROM/PROM Storage for Firmware Programs**
- **2K and 4K Banks Provide Flexibility**
  - 8- or 16-bit Memory Word Size
- **Switch Select Memory Addressing for Easy System Integration**
- **Variable Access Time for a Variety of 1702 PROM's**
- **Plug-replacement for SBC-406**

Product Overview

The BLC-406 6K byte Read Only Memory Board is designed for use in applications requiring non-volatile fixed programs (firmware). The BLC-406 extends any BLC/SBC microcomputer's on-board read only memory, leaving the on-board RAM available for scratch pad or transient operations.

A completely populated BLC-406 board requires 24 modules using National's MM1702A or MM1302 PROM/ROM type circuits. Sockets for the modules are provided on the board.

The BLC-406 is a plug-replacement for Intel's SBC-406.

Functional Description

The BLC-406 is organized in two read only sections, a 4K byte array and a 2K byte array. Up to 24 MM1702A Programmable Read Only Memory (PROM) or MM1302 Read Only Memory (ROM) modules may be installed. A 2K byte array requires 8 ROM/PROM modules while a 4K byte array requires 16.

Access time is a function of the particular ROM/PROM modules used and ranges between 1 and 2.5 microseconds. Timing control circuits on the BLC-406 permit synchronization with the particular ROM/PROM timing characteristics.

The 8-bit byte memory word length may be changed to a 16-bit word length using on-board jumpers. 2K words are available when the BLC-406 is used as a 16-bit word memory.

On-board switches allow user selection of address assignment. The 4K and 2K byte address blocks may be independent or double assigned for a 16-bit word configuration. Addresses may be assigned on any 2K byte boundary within the 64K byte system address range.

Specifications

Memory Size —	6K bytes (8-bit) 2K words (16-bit)
Word Size —	8 or 16 bits
Access Time —	Variable, 1 to 2.5 microseconds
Address Selection —	Jumper selection of contiguous 2K byte blocks
System Bus Interface —	All address, data and control signals are TRI-STATE™ compatible
System Bus Connection —	86 contact double-sided card cage edge connector on 0.156 inch centers
Compatible Memory Modules —	MM1302 ROM MM1742 ROM MM1702 PROM
Power —	+5V, 2.5A −10V, 1.45A
Environmental —	Temperature 0° to 55°C Humidity 0 to 90%, non-condensing

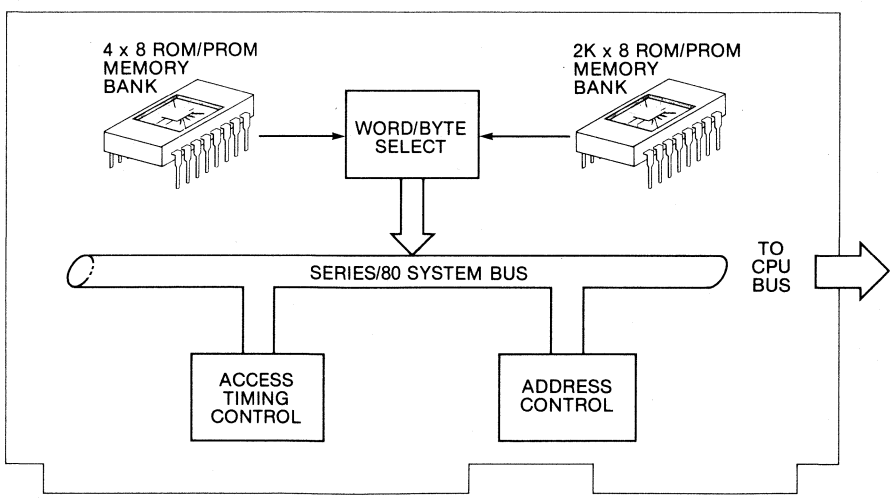
Physical —			
	Height	6.75 in.	(17.15 cm)
	Width	12.00 in.	(30.48 cm)
	Depth	0.50 in.	(1.27 cm)
	Weight	12 oz.	(340.2 g)

Order Information

BLC-406	6K Byte Read Only Memory Board contains sockets for independent 4K and 2K byte banks of ROM/PROM modules

Documentation

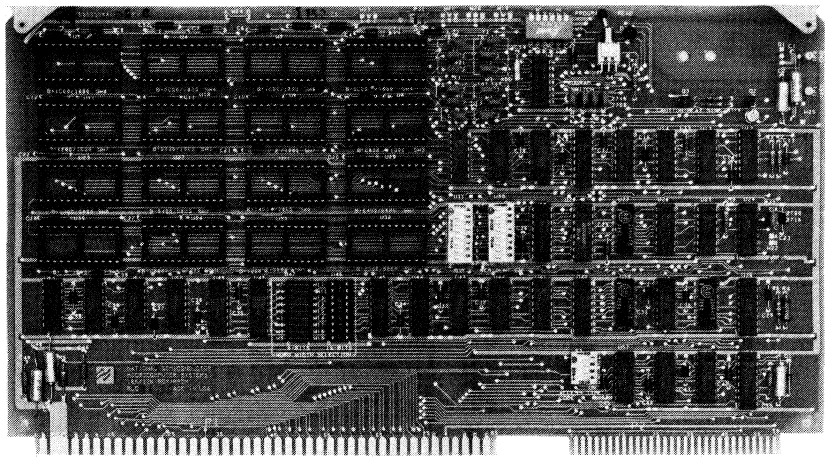
420305374-001	BLC-406 6K Byte ROM Board Hardware Reference Manual.



BLC-406 Diagram

National Semiconductor

BLC-416 and BLC-8432 16K and 32K ROM/PROM Boards



- **Complete System Flexibility**
  - Jumper options select MM2308/2708 or MM2316E/2716 devices, allowing twice the standard memory capacity
  - Selectable base addressing for independent 4K/8K blocks
  - Individual 1K/2K block enable/disable
  - On-board programming for MM2716 devices
  - Space for −5V regulator
- **Ease of Use**
  - Buffered address and data lines
  - Fully TTL compatible
- **Fully Compatible with Industry Standard BLC/SBC Series/80 Family of Microcomputer Products**
  - Plug-replacement for SBC-416

Product Overview

The BLC-416 and BLC-8432 ROM/PROM Boards provide highly flexible, low cost, read only memory expansion for Series/80 Board Level Computers. The fully expanded board may contain 16K or 32K bytes of ROM or EPROM depending on the modules installed. The BLC-416 and BLC-8432 plug directly into any Series/80 backplane or system and the BLC-416 is a direct replacement for the 16K byte SBC-416.

The BLC-416 and BLC-8432 provide the capability to program MM2716 EPROM's directly. This feature eliminates the need for a separate PROM programmer in OEM systems.

To maintain compatibility with MDS systems not containing a −5V power bus, a low cost regulator may be installed on the board to provide −5V power to the PROM's.

Functional Description

A set of switches and user-selectable BERG™ jumpers on the BLC-416 and BLC-8432 enable 1K or 2K memory block increments and allow base address selection of independent 4K or 8K blocks of memory beginning on any 4K/8K boundary, depending upon the type of memory device installed.

Four easily accessible switches located at the user interface edge of the board allow for timing adjustments when ROM/PROM's overlap RAM. Two other switches are used for disabling 8K or 16K blocks to allow maximum configuration flexibility and memory space allocation.

Full interface and timing logic is provided to allow on-board programming of MM2716 devices. Where a programming voltage of +25VDC is applied through the auxiliary connector, the user can

program any device simply by issuing memory reference instructions from the system CPU. A status indicator and switch on the board display the mode of operation and thus prevent accidental programming.

Specifications

Memory Capacity —	BLC-416	16K bytes in 1K increments
	BLC-8432	32K bytes in 2K increments
Word Size —	8 bits (16-bit jumper selected option)	
Compatible Memory Devices —	MM2308 ROM MM2708 EPROM MM2316E ROM MM2716 EPROM	
Address Selection —	2308/2708 devices — 4K banks on 4K boundaries 2316E/2716 devices — 8K banks on 8K boundaries	
System Bus Interface —	Address, control, and data lines are TRI-STATE™ TTL compatible	
Connectors —		
System Bus	86 contact double-sided card cage edge connector on 0.156 inch centers	
Auxiliary	60 contact double-sided edge connector on 0.1 inch centers Recommended mating connector: AMP P35-14559 TI H311130	

Power —	VDC	Fully loaded 2708 EPROM's	Fully loaded 2716 EPROM's
	+5V	0.01 A	1.40 A
	−5V	0.72 A	—
	+12V	1.04 A	—
	−12V	—	—
	−25V ± 1V (Programming Voltage)	—	0.12 A

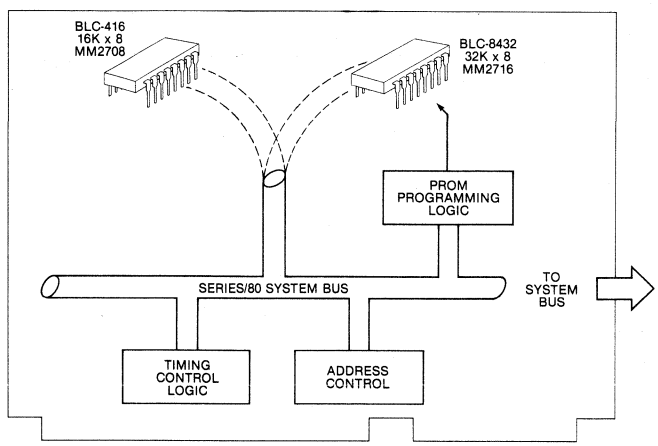
Environmental —	Temperature 0° to 55°C		
	Humidity 0 to 90% non-condensing		
Physical —	Height	6.75 in.	(17.15 cm)
	Width	12.00 in.	(30.48 cm)
	Depth	0.50 in.	(1.27 cm)
	Weight	12 oz.	(340.2 g)

Order Information

BLC-416	ROM/PROM Expansion Board factory configured for 2308/2708 devices. Sockets provide a total of 16K bytes of memory.
BLC-8432	ROM/PROM Expansion Board factory configured for 2316E/2716 devices. Sockets provide a total of 32K bytes of memory.

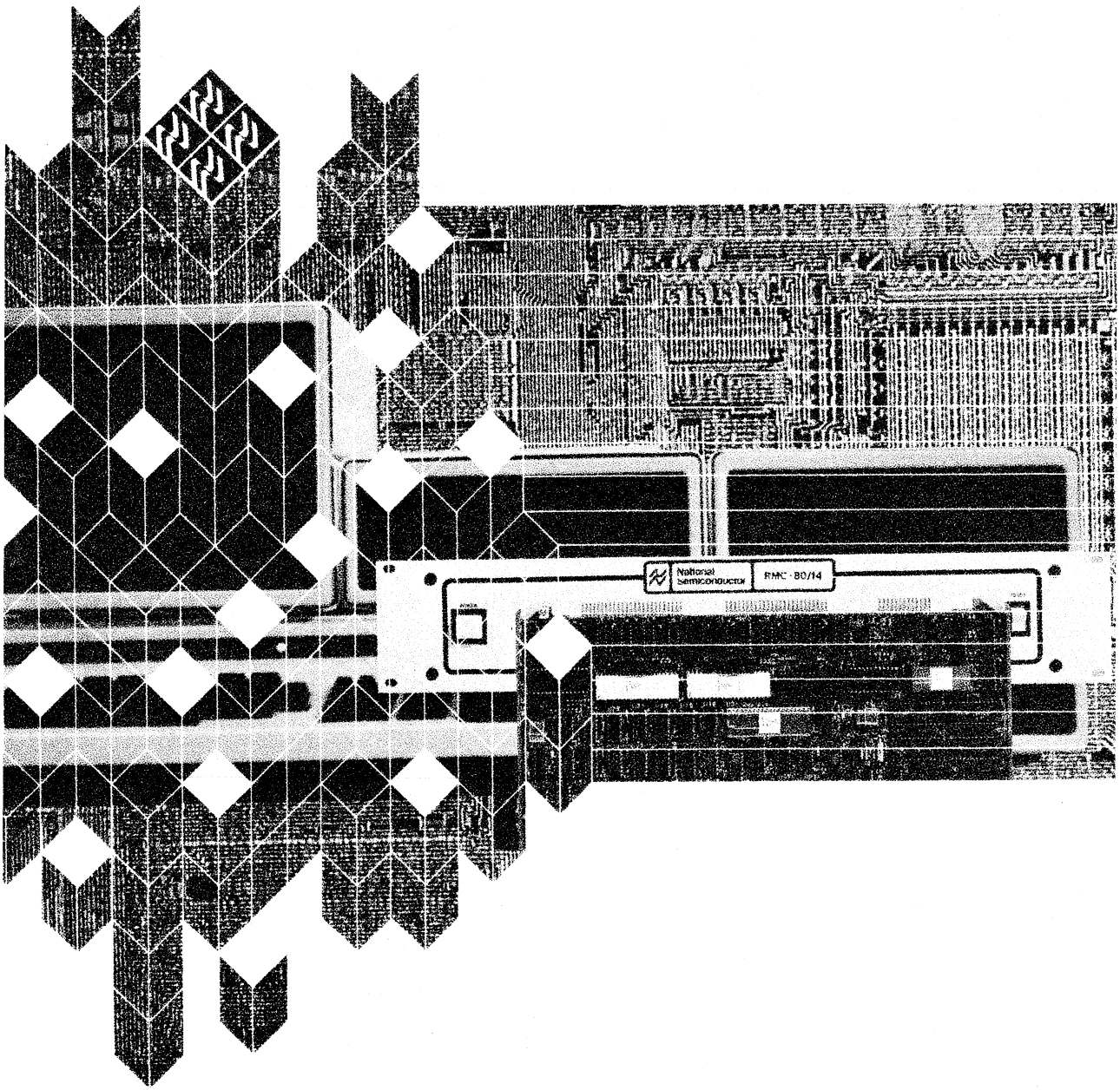
Documentation

420305447-001	BLC-416/8432 16K/32K ROM/PROM Board User's Manual



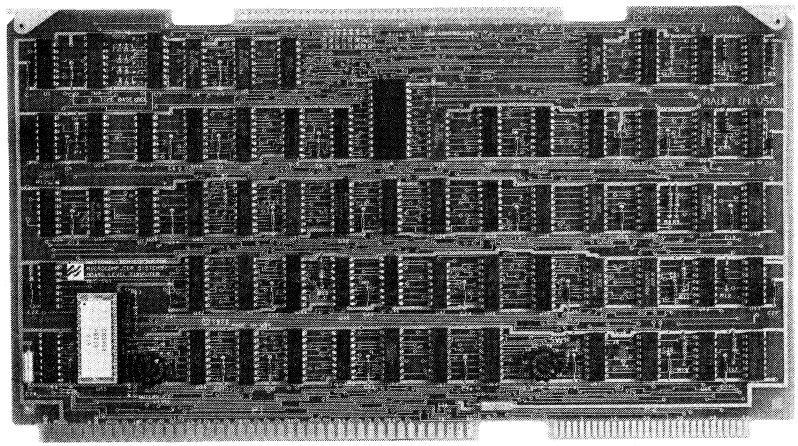
BLC-416 and BLC-8432 Diagram

Section 5
Input/Output
Expansion Boards



National Semiconductor

BLC-501
Direct Memory Access Board



- **Design Flexibility**
  - Interleaved mode data transfer rate up to 330K bytes per second
  - Burst mode data transfer rate up to one million bytes per second
  - Data block transfer length up to 64K bytes
  - Interrupt priority switch selectable to 8 levels
- **Multiprocessor System Capabilities**
  - Bus master capability
  - Software selectable/maskable interrupt operations
  - Memory addressing to 64K locations, software initialized transfers
- **Industry Standard**
  - Bus control logic permits use with all BLC/SBC board level computers
  - Plug-replacement for SBC-501

Product Overview

The BLC-501 Direct Memory Access (DMA) Controller Board complements the broad line of Series/80 products by providing the capability for high speed data transfers between input/output devices and system expansion memory. The DMA board significantly enhances the flexibility of system design with multiple transfer modes and control capability for up to 16 independent devices. The interleaved transfer mode permits data transfers at a maximum rate of 330K bytes per second, while the burst mode permits transfers at a maximum rate of one million bytes per second for high speed applications.

The BLC-501 is fully compatible with BLC/SBC microcomputers and interfaces directly with the system bus for data communication and control. The DMA controller takes full advantage of Series/80 architecture and permits data transfers into the full 64K byte memory range.

Functional Description

The BLC-501 can operate in either the interleaved or the burst data transfer mode.

In the interleaved data transfer mode the DMA controller shares the system bus with the CPU. Each time the DMA controller gains control of the bus, a byte is transferred. In this way the CPU uses the bus on an interleaved basis with the DMA controller. The maximum data transfer rate in this mode is 330K bytes per second.

The burst data transfer mode is employed when maximum data transfer rate is necessary. In this mode, the DMA controller holds the system bus for the entire length of the data block. The maximum data transfer rate in this mode is one million bytes per second. Bus control logic is incorporated to permit use with all Series/80 Board Level Computers. This logic allows the CPU to regain control of the system bus upon completion of data transfer.

The BLC-501 DMA controller is capable of transferring data in 16-bit parallel word size when used with 16-bit word memory modules.

Standard Series/80 instructions control the BLC-501. Output parameters are defined in Table I, input parameters in Table II. Sixteen contiguous addresses are used by the DMA controller. Switch selection is allowed within the range 00_{16} to $F0_{16}$. There are five status and control registers in the BLC-501 DMA board:

- 6-Bit Control Register — Specifies the word size, the busy status, the type of operation to be performed, the data transfer direction, the state of the interrupt system, and the DMA bus usage mode.
- 16-Bit Memory Address Register — Specifies the 16-bit address of the memory location to be accessed. For multiple word transfers, this register is incremented by one after each word has been transferred.
- 16-Bit Length Register — Specifies the unsigned binary value of the total number of words to be transferred (up to 64K). For multiple word transfers, this register is decremented by one after each word has been transferred. Transfers are halted when the length register equals zero.
- 4-Bit Tag Register — A general purpose register that can be used as a command/control register for external devices. With the addition of external decoding logic, up to 16 devices can be interfaced to the BLC-501. To control data transfers, a total of 8 program selected and initiated command strobes are provided — 4 for input and 4 for output. Strobe widths are selected by means of jumpers. Available widths are 100, 200, 400, 800 or 1600 ns.
- 8-Bit Status Register — Provides 4 bits of internal controller status: program interrupt, memory read/write, interrupt status, and controller busy. The remaining 4 bits provide status information from user supplied external devices.

Interrupt requests are passed to the system CPU on one of 9 switch-selected priority levels. These requests may be automatically generated when a data transfer operation is completed (byte for interleaved mode or block for burst mode), when an external device signals an interrupt, or for test purposes. Interrupt enable is program controlled, allowing a high degree of user flexibility.

Table I. Output Parameters

Address	Parameter
Base + 0	Output strobes to external devices
Base + 1	
Base + 2	
Base + 3	
Base + 4	
Base + 5	Not used
Base + 6	
Base + 7	
Base + 8	Set the "SET INT" latch (also sets the INT latch if DMA not busy)
Base + 9	Clears interrupt, DMA busy and SET INT latches
Base + A	Load control register
Base + B	Load tag register
Base + C	Load least significant byte of length register
Base + D	Load most significant byte of length register
Base + E	Load least significant byte of memory address register
Base + F	Load most significant byte of memory address register

Table II. Input Parameters

Address	Parameter
Base + 0	Input strobes to external devices
Base + 1	
Base + 2	
Base + 3	
Base + 4	Read least significant byte
Base + 5	Read most significant byte
Base + 6	Read DMA status word
Base + 7	Input strobe to external devices
Base + 8	Not used
Base + 9	
Base + A	
Base + B	
Base + C	
Base + D	
Base + E	
Base + F	

Specifications

Maximum I/O Data Rates —	One million bytes per second (burst) 330K bytes per second (interleaved)
Maximum Number of Devices —	16
Data Transfer Format —	8-bit parallel or 16-bit parallel
Direct Memory Access Method —	Bus master for burst mode Cycle steal for interleaved mode
Address Range —	64K bytes
System Bus Interface —	Data, address and command signals are TRI-STATE™ TTL compatible
Device Interface —	TTL compatible, 48 milliamp sink capability using 150 ohm termination

Connectors

System Bus	86 contact double-sided card cage edge connector on 0.156 inch centers
Auxiliary	60 contact double-sided edge connector on 0.1 inch centers Recommended mating connector: 3M "Scotchflex" 3463-0001
Device	100 contact double-sided edge connector on 0.1 inch centers Recommended mating connectors: Arco AI150WP11 or AE150WP21 Elco 006307100472001 CDC VPB01B50A00A1

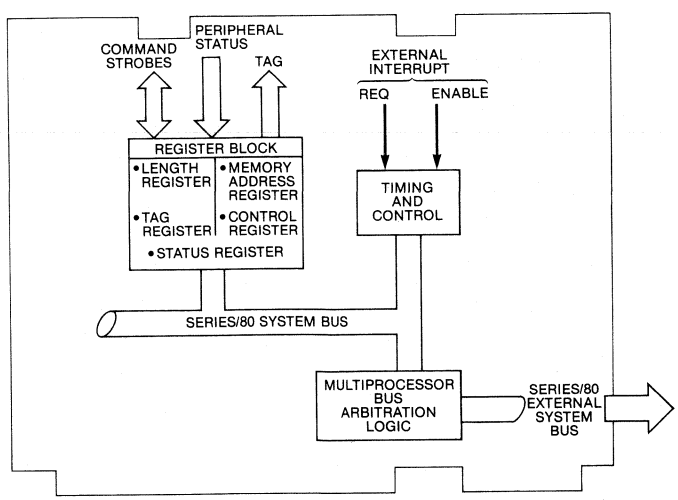
Power —	+5V, 3.35A		
Environmental —	Temperature 0° to 55°C Humidity 0 to 90% non-condensing		
Physical —	Height	6.75 in.	(17.15 cm)
	Width	12.0 in.	(30.48 cm)
	Depth	0.5 in.	(1.27 cm)
	Weight	14.0 oz.	(396.9 g)

Order Information

BLC-501	Direct Memory Access Board

Documentation

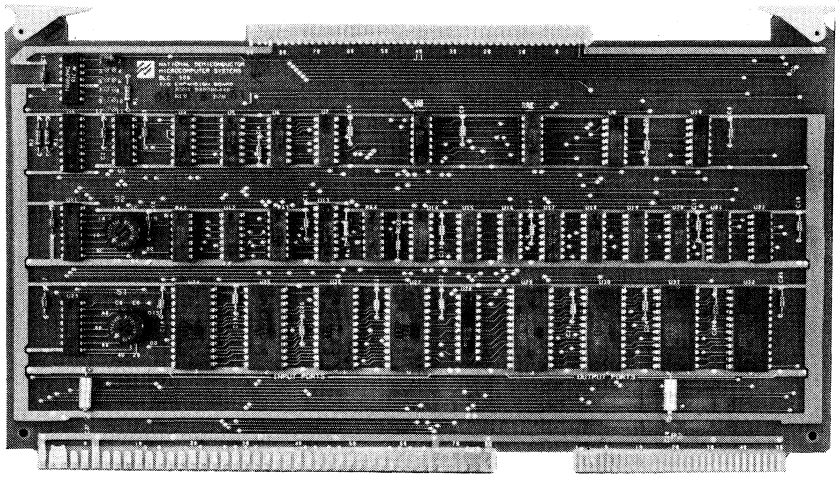
420305525-001	BLC-501 Direct Memory Access Board Hardware Reference Manual



BLC-501 Diagram

National Semiconductor

BLC-508
Input/Output Expansion Board



- **Independently Controlled 8-bit Parallel Ports**
  - Four input ports
  - Four output ports
- **Variable Width Strobed Outputs Permit Synchronization with External Devices**
- **Interrupts for Reduced System Overhead Control**
  - Automatic input port interrupt
  - Eight external available
- **Switch Selected Port Address for System Integration Flexibility**
- **Plug-replacement for SBC-508**

Product Overview

The BLC-508 Input/Output Expansion Board is specifically designed as an economical solution for limited digital input/output application requirements where system computer input/output line capacity is exhausted.

The BLC-508 provides four 8-bit input ports and four 8-bit output ports, each individually addressable. Input and output operation is governed by an on-board strobe with a variable interval to meet a variety of external timing requirements.

The BLC-508 is a plug-replacement for Intel's SBC-508 board.

Functional Description

Input

The input section contains four independent 8-bit ports. Incoming data is latched or unlatched in the input buffer. A buffer full interrupt may be generated to the system CPU to signal data availability.

TRI-STATE™ TTL compatible 8212 devices permit interfacing to a wide range of external devices. Input lines are terminated with 1K ohm pull-up resistors contained in 14-pin DIP modules and mounted in on-board sockets.

Output

The output section contains four independent 8-bit ports. Data is presented to the output port using an I/O write command from the system CPU. Output data is latched in the output buffer. The output strobe to the external device signals the device that data is available.

TRI-STATE™ TTL compatible 8212 devices are used to permit interfacing to a wide range of external devices. Each output line is capable of driving a 48 milliamp load.

The output strobe is variable to permit synchronization with the peripheral device requirements. The strobe pulse width may be jumper selected to 100, 200, 400, 800 or 1600 nanoseconds.

Interrupts

In addition to the interrupt logic associated with the input ports, the BLC-508 contains 8 line external interrupt control. The interrupt driven I/O control feature may be implemented in one of two ways: as a discrete interrupt level or as a single level multi-sourced interrupt. Interrupts are automatically cleared after servicing.

Addressing

Input and output ports use eight contiguous addresses. The base address is the lowest of the eight and is selected by on-board switches. This permits a high degree of system integration flexibility.

Specifications

Number of Input Ports —	4
Number of Output Ports —	4
I/O Port Data Width —	8-bit
I/O Buffer Mode —	Latched
Input Termination —	1K ohm
Output Drive —	48 ma
Output Strobe Width —	Variable 100, 200, 400, 800 or 1600 ns
External Interrupt Capacity —	8
System Bus Interface —	Data, address and command signals are TRI-STATE™ TTL compatible.

Connectors

System Bus	86 contact double-sided card cage edge connector on 0.156 inch centers
Input/Output	100 contact double-sided edge connector on 0.1 inch centers Recommended mating connector: Arco AE150WP11 AE150WP21 Eko 006307100472001 CDC VPB01B50A00A1

Power —	+5V, 2.2A
Environmental —	Temperature 0° to 55°C Humidity 0 to 90% non-condensing

Physical

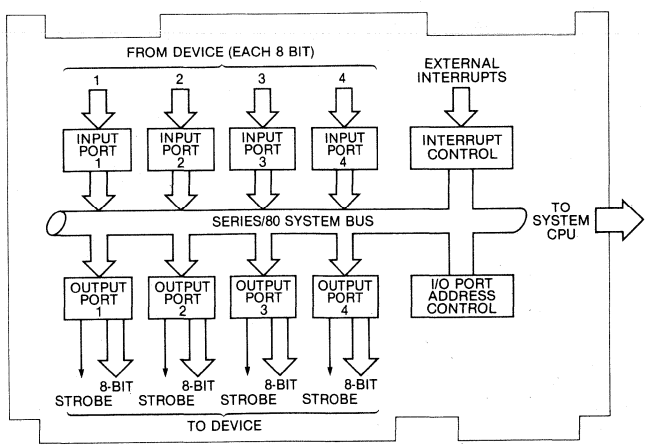
Height	6.75 in.	(17.15 cm)
Width	12.00 in.	(30.48 cm)
Depth	0.50 in.	(1.27 cm)
Weight	12 oz.	(340.2 g)

Order Information

BLC-508	Input/Output Expansion Board. Contains 8 independent input and output 8-bit parallel ports.

Documentation

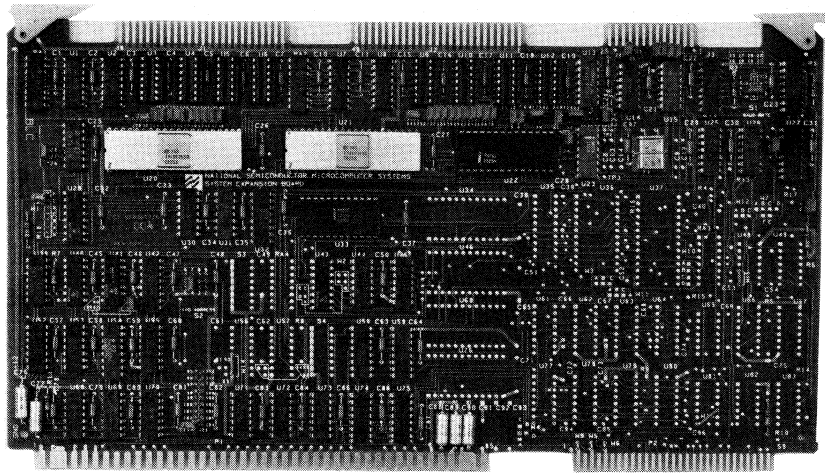
420305448-001	BLC-508 Input/Output Board Hardware Reference Manual



BLC-508 Diagram

National Semiconductor

BLC-517
Input/Output Expansion Board



- **48 Programmable Input/Output Lines for Digital Control Applications**
- **Synchronous/Asynchronous Serial Channel Permits Data Communication Interfacing to Data Set or Data Terminal**
- **Baud Rates of 75 to 38.4K Allow Interfacing to Broad Range of Serial Input/Output Devices**
- **8 Maskable Interrupts for Easy System Control**
- **1 Millisecond Interval Timer for Automatic Time Controlled Sequences**
- **Compatible with BLC/SBC Series/80 Software and Hardware**
- **Plug-replacement for SBC-517**

Product Overview

The BLC-517 Combination Input/Output Expansion Board complements the broad range of BLC/SBC Series/80 Board Level Computers with digital input/output expansion capability.

Both parallel and serial input/output are provided: 48 programmable parallel lines and one synchronous/asynchronous serial port. The 48 line programmable input/output capability may be configured to provide a variety of unidirectional and bidirectional combinations. The serial channel is capable of data transmission rates of up to 38.4K baud. Maskable interrupts and a one millisecond timer are included to provide complete system control.

The BLC-517 is a plug-replacement for Intel's SBC-517.

Functional Description

Parallel Input/Output

The 48 input/output lines are controlled by two INS8255 Programmable Peripheral Interface Circuits. Using standard Series/80 instructions, the 48 lines may be configured to a variety of 4 and 8 parallel line segments capable of latched or unlatched operation in unidirectional and bidirectional modes. The parallel input/output is divided into six ports, each containing 8 bits.

Three basic modes of operation may be selected by program instructions:

- Data read or write to the specified port without the use of handshake signals. Output data is latched while input data is unlatched.

- Data read or write to the specified port using strobe or handshake signals created by or transmitted to the interfaced external device.
- Data read or write to the specified port using a bidirectional port to communicate with the external device. Handshake signals are provided by a separate "control" port (port 3 or 6).

Input/output modes for all ports are defined in Appendix B.

Sixteen input/output lines have 8226 type bidirectional drivers and terminators permanently installed. The remaining 32 lines are fitted with sockets to permit user selection of drivers and terminators to match specific line characteristics. Line driver and terminator circuits are contained in 14 pin DIP packages.

National's BLC-901 and BLC-902 terminator modules are available as options to satisfy termination requirements. The BLC-901 contains 220/330 ohm divider type circuits for four lines, while the BLC-902 contains 1K ohm pull-up type terminator circuits for four lines. Figure 1 illustrates the terminator circuit configuration.

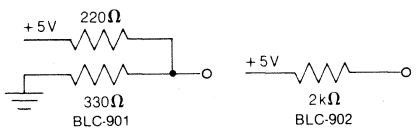


Figure 1. BLC-901 and BLC-902 Terminators

A variety of TTL compatible driver circuit types is available: inverting, non-inverting, high voltage and open collector combinations with sink current capacity ranging from 16 to 48 milliamps. (See Table I.)

Table I. Drivers

Type	Output	Current (ma)
7400	I	16
7403	I, OC	16
7408	NI	16
7409	NI, OC	16
7426	I, OC, HV	16
7432	NI	16
7437	I	48
7438	I, OC, HV	48

(I = inverting; NI = non-inverting; OC = open collector; HV = high voltage)

Serial Input/Output

The serial I/O port control is based on a Universal Synchronous/Asynchronous Receiver/Transmitter (USART) circuit. The port is fully EIA RS232C compatible, thereby allowing interface with a wide range of data sets and data terminals. Standard Series/80 instructions control data transmission, and software is used to implement the desired transmission protocol technique. The port is double buffered for full duplex transmissions and contains full data set control to and from modems. Character framing and transmission mode parameters are controlled by programmable features and jumpers.

Synchronous transmission features:

- 5-, 6-, 7- or 8-bit characters
- Automatic SYNC character insertion, 1 or 2 characters
- SYNC search
- External synchronization
- Even or odd parity

Asynchronous transmission features:

- 5-, 6-, 7- or 8-bit characters
- Odd, even or no parity
- 1, 1½ or 2 stop bits
- False start bit detect
- Break character generation

Baud rate may be selected from the range 75 through 38.4K. Table II lists the rates available for synchronous and asynchronous data transmission. Three baud rates, based on a multiple of X1, X16 or X64 of the basic frequency, are program selectable.

Table II. Baud Rates

Synchronous	Asynchronous	
6980	75	1200
4800	110	2400
9600	150	4200
19200	300	9600
38400	600	19200

Error and status conditions are presented in the status word. Error condition may result from a framing error, data overrun (new character arrives before the buffer is empty) or incorrect data parity. Figure 2 illustrates the status word.

7	6	5	4	3	2	1	0
Data Set Ready	Sync Detect	Framing Error	Data Overrun	Parity Error	Transmit Enable	Ready to Receive	Ready to Transmit

Figure 2. Status Word

The RS232C serial port may be converted to 20 ma current loop operation with an optionally available BLC-530 Current Loop Adapter. This permits interfacing devices such as teletypewriters, video displays and others not containing an RS232C compatible interface.

Interrupts

The BLC-517 is designed to handle up to eight interrupt requests. Four may be jumper selected to permit automatic interrupt when a parallel character is received from or output to an external device.

Two interrupts may be configured to signal serial port character received and character transmitted.

The two remaining interrupt lines are shared by the 1 millisecond interval timer and two external event signal inputs.

The eight interrupts may be OR tied to form a single interrupt line to a system processor such as a BLC-80/10, or may be discrete when used with a system processor such as a BLC-80/204.

The eight interrupts may be individually masked under program control. The status of the interrupts is available to the system via the mask register.

Addressing

The BLC-517 uses 16 contiguous addresses. The base, or board, address is jumper selectable to permit a high degree of system integration flexibility.

Specifications

Parallel Input/Output

Number of Ports — 6

Number of Lines — 48

Configuration — Single, 4- or 8-bit

Data Transfer Modes — Unidirectional and bidirectional

Data Control — Latched, unlatched and strobed

Interface — TTL compatible

Compatible I/O Driver Modules —

Type	Output	Current (ma)
7400	I	16
7403	I, OC	16
7408	NI	16
7409	NI, OC	16
7426	I, OC, HV	16
7432	NI	16
7437	I	48
7438	I, OC, HV	48

(I = inverting; NI = non-inverting; OC = open collector; HV = high voltage)

Compatible I/O Termination Modules — BLC-901 220/330 ohm divider
BLC-902 1K ohm pull-up

Serial Input/Output

Control — Programmable USART

Transmission Modes — Synchronous and asynchronous

Character Length — 5-, 6-, 7- or 8-bit

Parity — Odd, even or none

SYNC Functions — SYNC search
Automatic 1 or 2 SYNC character insertion

Asynchronous Stop Bits — 1, 1½ or 2

Asynchronous Break — Programmable control generation

Baud Rates — (asynchronous program controlled)

75	2400
110	4800
150	6980
300	9600
600	19200
1200	38400

External SYNC Control — Yes

Error Detection — Framing
Data overrun
Parity

Interface — RS232C

Interrupt — 8 lines
Program maskable
Discrete/OR tie capability

Timer 1 millisecond intervals

System Bus Interface

All address, data and control signals are TRI-STATE™ TTL compatible.

Connectors

System Bus — 86 contact double-sided card cage edge connector on 0.156 inch centers

Auxiliary — 60 contact double-sided edge connector on 0.1 inch centers

Recommended mating connector:
CDC VPB01B30A00A2
AMP PES-14559
TI H311130

Parallel I/O — 50 contact double-sided edge connector on 0.1 inch centers

Recommended mating connector:
3M 3415-001
AMP 2-86792-3

Recommended cables:
BLC-956 Parallel I/O Cable Kit (two 5 foot ribbon cables)

Serial I/O 26 contact double-sided edge connector on 0.1 inch centers

Recommended mating connector:
3M 3462-0001 flat
AMP 1-583715-1 round

Power +5V, 2.4A
+12V, 0.04A
−12V, 0.06A

Environmental Temperature 0° to 55°C
Humidity 0 to 90% non-condensing

Physical

Height	6.75 in.	(17.15 cm)
Width	12.00 in.	(30.48 cm)
Depth	0.50 in.	(1.27 cm)
Weight	14 oz.	(396.9 g)

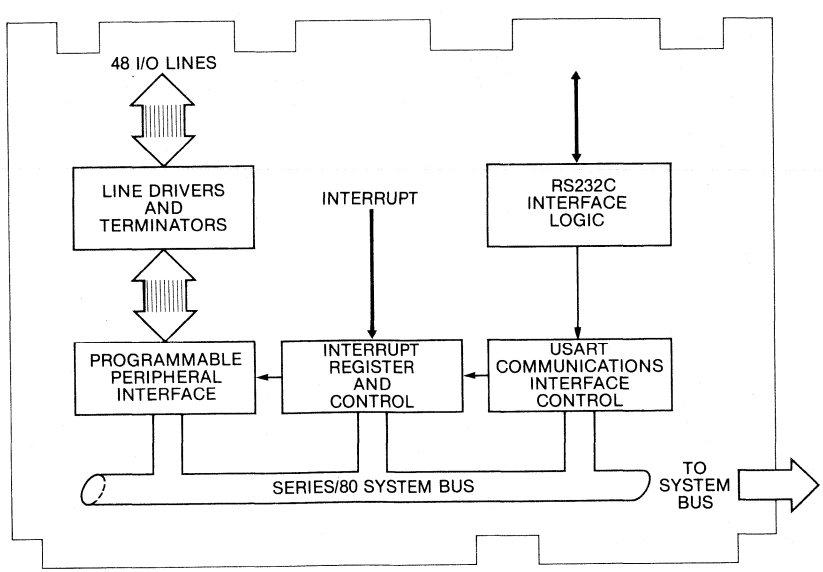
Order Information

BLC-517 Input/Output Expansion Board
Contains 48 parallel and one serial programmable I/O lines, interrupt capability and 1 millisecond interval timer.

BLC-956 Parallel I/O Cable Kit
Contains two 5 foot ribbon cables for connection to parallel input/output board edge connectors.

Documentation

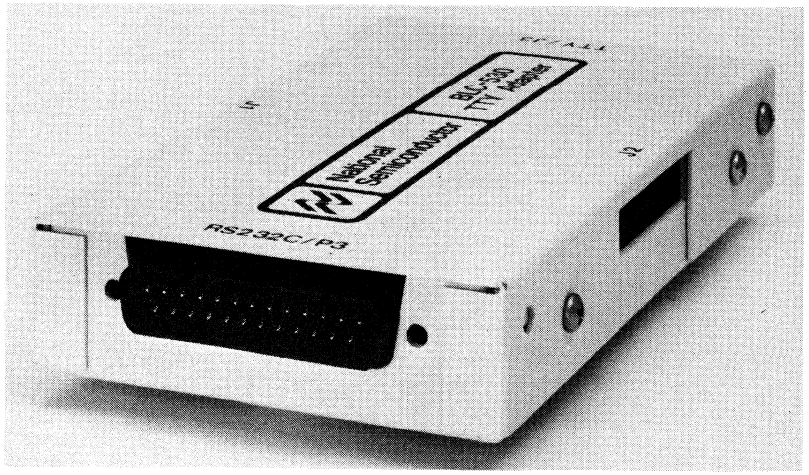
420305376-001 BLC-104/116/517 Input/Output and Memory Expansion Boards Hardware Reference Manual



BLC-517 Diagram

National Semiconductor

BLC-530
Current Loop Adapter



- **Current Loop Conversion for RS232C Serial I/O Channels Extends Series/80 Capability**
- **Data Set or Data Terminal Configuration for Application Flexibility**
- **Baud Rate of up to 9600 Allows Wide Range of Interface Applications**
- **Fully Compatible with BLC/SBC CPU's and I/O Expansion Boards**
- **Plug-replacement for SBC-530**

Product Overview

National's BLC-530 Current Loop Adapter provides an ideal low cost solution for converting an RS232C serial input-output channel to a 20 milliamperes current loop mode.

Designed in anticipation of the need for application flexibility, the BLC-530 may be used with Series/80 microcomputer and I/O boards when connection is made between the computer and a current loop device, between the computer and a data set, or between a data set and a current loop device.

The BLC-530 easily accommodates a wide variety of applications. Its 9600 baud bandwidth simplifies selection criteria and minimizes the need to use several different types of adapters. The BLC-530 is housed in a small independent container and, thus, does not occupy valuable board slots. This can result in savings in system space and cost.

Fully plug-compatible with Intel's SBC-530, the National BLC-530 may be used with any Intel, National or equivalent Series/80 system.

Functional Description

The BLC-530 Current Loop Adapter is a passive device capable of responding to full or half duplex transmissions without reconfiguration. The line interface on the current loop side of the adapter is optically coupled to assure current loop and RS232C signal isolation.

Current for the current loop is derived from one of two sources. In the standard configuration the adapter derives power from the RS232C serial input-output port 12 volt source. Optionally, the user may reconfigure the adapter to allow power to be supplied from an independent source. A Molex connector is incorporated as an integral part of the adapter for this purpose. Configurations are simply and easily changed by repositioning BERG™ jumpers — no tools or wire are necessary.

The adapter contains two 25-pin connectors for interconnecting the RS232C and current loop channel. Inadvertent cable cross connection is prevented by using a socket-type connector for the RS232C side and a plug connector for the current

loop side. For short distance requirements the BLC-955 I/O Cable Kit is optionally available for use with the BLC-530. The cable kit consists of a 5 foot RS232C interface cable and a 2.5 foot current loop cable. The RS232C cable connector mates to the BLC-530 and to a Series/80 board serial I/O port edge connection. Pin signal assignments are listed in Table I.

Because the BLC-530 is completely self-contained in a separate container it does not require a card cage slot. Instead, the adapter may be located in any desired place and may be stacked. For mounting convenience, the container has threaded mounting holes.

Table I. BLC-530 Connector Pin Assignments

Pin	RS232C Signal	Current Loop Signal
1	Ground	Ground
2	Transmit Data	—
3	Receive Data	—
4	Request to Send	—
5	Clear to Send	—
6	Data Set Ready	—
7	Ground Carrier Detect	—
11	+12V	—
12	—	TTY Receive
13	Sec Clear to Send	TTY Transmit
14	Sec Transmit Data	—
15	Transmit Clock	—
16	Sec Receive Data	TTY Read Control
17	Receive Clock	—
19	Sec Request to Send	—
20	Data Terminal Ready	—
21	—	TTY Read Control Return
22	Ring Indicator	—
23	−12V	—
24	DTE Transmit Clock	TTY Receive Return
25	—	TTY Transmit Return

Specifications

Baud Rate — To 9600 Baud

Transmission Mode — Passive (Half or Full Duplex)

Interface Standard — EIA RS232C

Drive Current — 20 ma loop

Current Source — RS232C I/O Port (optionally from independent source)

Recommended Mating Connector — RS232C side: Cannon DB-25S or equal
Current Loop Side: Cannon DB-25P or equal
Independent Power: Molex 09-50-7071 with pins or equal

Maximum Current —

	+12V	−12V
RS232C side	30 ma	30 ma
Current Loop side	40 ma	40 ma

Environmental — Temperature 0° to 55°C
Humidity 0 to 90% non-condensing

Physical —

Height	4.85 in.	(12.32 cm)
Width	2.88 in.	(7.31 cm)
Depth	0.92 in.	(2.34 cm)
Weight	9 oz.	(255.2 g)

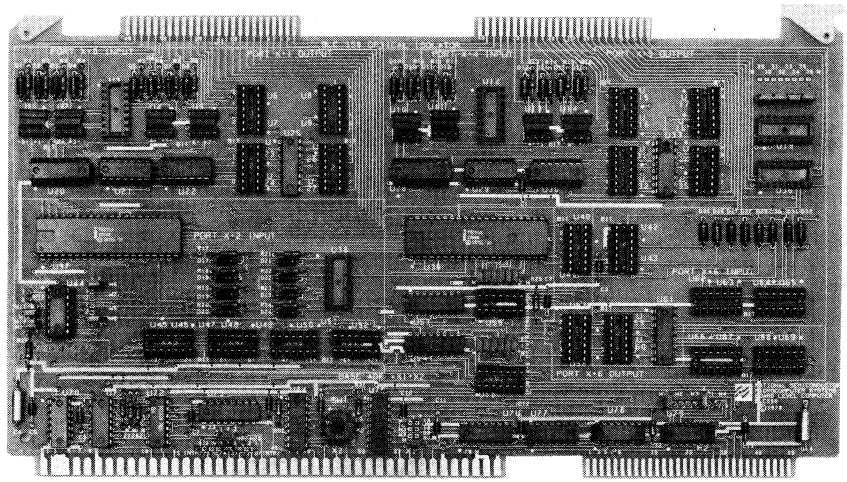
Order Information

BLC-530 Current Loop Adapter

BLC-955 I/O Cable Kit
Consists of one 5 foot RS232C serial I/O cable and one 2.5 foot current loop cable.

National Semiconductor

BLC-556
Optically Isolated Input/Output Board



- **Protects Series/80 System from External Voltages of Up to 500 VDC**
- **Eliminates Effects of Ground Loops by Optically Isolating 48 Digital I/O Lines**
- **Sockets for Custom Opto-Isolator Applications**
- **Sockets for I/O Line Drivers and Receivers to Suit User Requirements**
- **Jumper for User Selection of Interrupts**
- **Plug-replacement for SBC-556**

Product Overview

The BLC-556 is an optically isolated, programmable input/output board designed to provide complete isolation between the input/output device and the system computer. Typical applications of the BLC-556 include optical signal connectors to such devices as SCR's, TRIAC's, motors, solenoids and relays.

The board contains 48 program controlled data lines. The 48 data lines are configured into six parallel I/O ports of up to 8 lines per port.

The BLC-556 is a plug-compatible replacement for Intel's SBC-556.

Functional Description

The input/output operations are controlled using two INS8255 programmable peripheral interface modules. Each controls three parallel ports containing 8 lines each. These parallel ports are configured as follows:

- Three 8-line dedicated input ports
- Two 8-line dedicated output ports
- One programmable port configured as:
  - — 8-line input port; or
  - — 8-line output port; or
  - — 4-line input port and 4-line output port

The Series/80 Microcomputer communicates with the BLC-556 using standard input and output instructions. Eight contiguous addresses permit selection of a specific parallel port with the base address switch selectable. Address bits 3 through 7 specify the board base address and bits 0 through 2 identify a specific port on the selected board.

Table I. Input/Output Configuration

Port	1	2	3	Control	4	5	6	Control
Address	Base + 0	Base + 1	Base + 2	Base + 3	Base + 4	Base + 5	Base + 6	Base + 7
Mode	Input	Output	Input	Control Word	Input	Output	Input/ Output	Control Word

In addition to the 48 I/O lines, 8 interrupt lines can be connected to the Series/80 bus interrupt lines. Four external events may be tied to Port 3, Port 6, or both. Before servicing the interrupt, the CPU must read both ports 3 and 6 to identify the interrupting device.

The BLC-556 is designed to accept either differential or single-ended signal sources. The input voltage range is determined by the optical isolator selected and installed. The maximum isolation (limited by board breakdown and tolerances) is:

- Line-to-Line Isolation
  — 230 volts DC or Peak AC
- Input/Output Isolation
  — 500 volts DC or Peak AC

The user has complete freedom within the voltage ranges listed to select and install optical isolators specifically suited to the application. Sockets are provided for easy installation of DIP style circuits. Sockets are also provided for user-installed I/O terminators, input resistor packs and output drivers.

Specifications

I/O Ports — 6

I/O Lines — 48

Input — Single-ended
Differential

Isolation Limit — Line-Line: 230 VDC or Peak AC
I/O: 500 VDC or Peak AC

Recommended Opto-Isolators — Output: 4-pin DIP, LITRONIX ISO-LIT A-30
8-pin DIP, LITRONIX ISO-LIT CT6

System Bus Interface — Address, data and command signals are TRI-STATE™ TTL compatible

System Bus Connector — 86 contact double-sided card cage edge connector on 0.156 inch centers

Input/Output — 50 contact double-sided edge connector on 0.1 inch centers
Recommended mating connector:
3M 3415-001
AMP 2-86792-3

Power — +5V, 1.6A

Environmental — Temperature 0° to 55°C
Humidity 0 to 90% non-condensing

Physical —

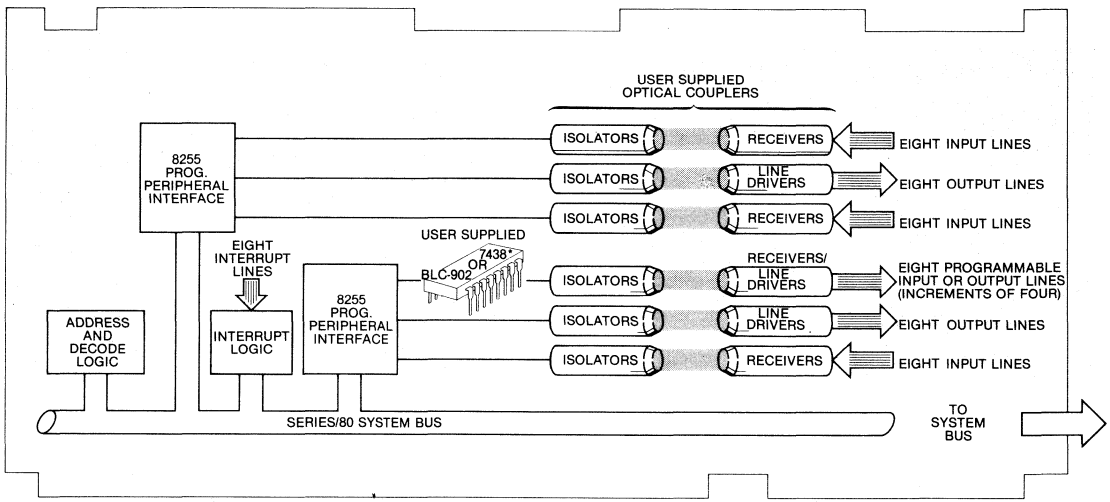
Height	6.75 in.	(17.15 cm)
Width	12.00 in.	(30.48 cm)
Depth	0.50 in.	(1.27 cm)
Weight	12 oz.	(340.2 g)

Order Information

BLC-556 Optically Isolated I/O Board

Documentation

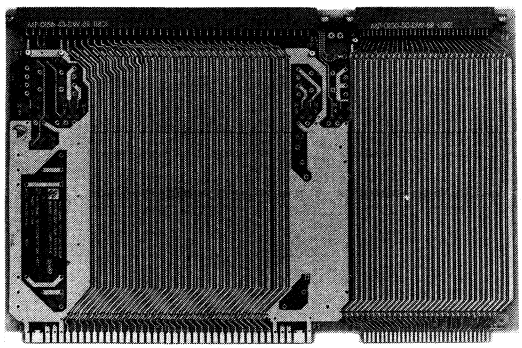
420305559-001 BLC-556 Optically Isolated I/O Board Hardware Reference Manual

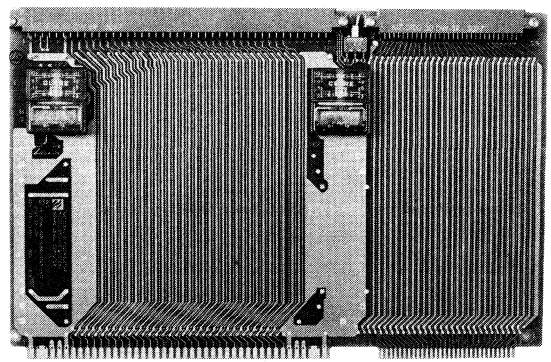


BLC-556 Diagram

National Semiconductor

BLC-610 and BLC-8610 Extender Boards





- **Power Isolation in BLC-8610 Allows Removal/Insertion of Boards without Loss of Data or Functions**
- **Easily Accessible Test Points for Fast Bus and Control Signal Examination**
- **Complete Access to a Series/80 Board for Troubleshooting or Debugging**
- **BLC-610 is Plug-replacement for Intel's MDS-610**

Product Overview

The BLC-610 and BLC-8610 Extender Boards may be used to extend Series/80 family form factor boards beyond the card cage for testing, trouble-shooting or customer debugging.

Each of these boards meets specific user needs: the BLC-610 provides pin-to-pin extension of the BLC-604 or BLC-614 Card Cage backplane and is fully compatible with the Intel SBC-610; the BLC-8610 retains form, fit and function compatibility with the BLC-610 but adds the dimension of power isolation control.

Power isolation enables the user to remove or insert the board under examination without powering down the entire system and losing instruction functions, status, valuable RAM-stored data, etc. Instead, simply flick the power control switch on the BLC-8610 to remove the power bus from the board being examined.

Test points are visible and easily accessible for examination of all backplane signals and power planes.

Functional Description

When installed in a BLC-604 or BLC-614 Card Cage, the BLC-610 provides uninterrupted feedthrough of each pin on backplane connectors J1 and J2 to a Series/80 board inserted in the BLC-610 connector.

The BLC-8610 contains the same features as the BLC-610 except that two relays are employed to allow the user to switch the power lines on and off, as desired, for testing or removal/insertion of Series/80 boards without fear of damage from transients. Power control does not affect the power supplied to the system except for the small amount of current necessary to drive the relays.

Both boards contain ground lugs tied to system ground via the ground bus from J1 and J2. These lugs are provided as a convenience for grounding test instruments.

Board current may be measured on the BLC-610 by removing jumpers and inserting meter probes used on power runs. On the BLC-8610, de-energized relays are "jumpered" and appropriate metering probes are then inserted on selected power runs.

Specifications

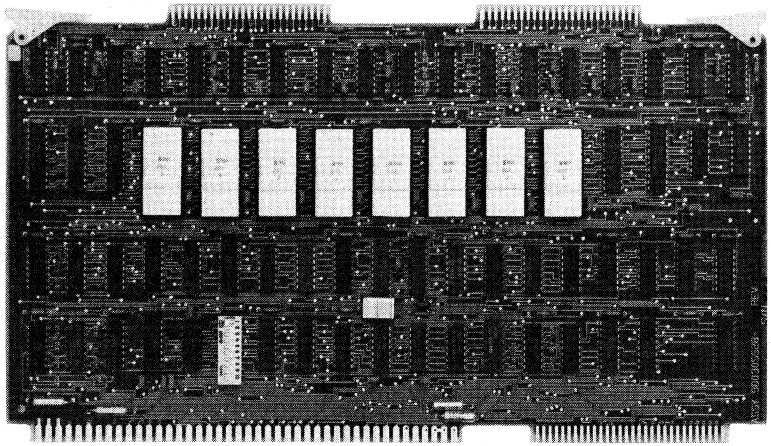
		BLC-610	BLC-8610
Current Rating —	+5V	20A	8A
	−5V	5A	2A
	−10V	5A	2A
	+12V	5A	2A
	−12V	5A	2A
Power —	BLC-610: None required BLC-8610: +12V, 60mA		
Environmental —	Temperature 0° to 55°C Humidity 0 to 90% non-condensing		
Physical —	Height	8.00 in.	(20.32 cm)
	Width	12.00 in.	(30.48 cm)
	Depth	0.50 in.	(1.27 cm)
	Weight	12 oz.	(340.2 g)

Order Information

BLC-610	Extender Board
BLC-8610	Extender Board with Power Control

National Semiconductor

BLC-8538
Eight Channel Communications Expansion Board



- **Full Software Parameter Control for Wide Range of Applications**
  - Asynchronous/synchronous
  - Data format and parity
  - Baud rates to 19.2K
  - Maskable interrupts
  - Modem control
- **Eight Independently Controlled Channels for Communications System Flexibility**
- **Error Detection for Each Channel**
- **Meets RS232C Interface Standards**

Product Overview

The BLC-8538 Eight Channel Communication Expansion Board is a member of National's Series/80 family and is specifically designed to provide flexible multichannel data communications capability for Series/80 BLC/SBC microcomputer systems.

The BLC-8538 provides fully independent programmable asynchronous or synchronous serial communication channels conforming to the EIA RS232C standard, thereby allowing connection to a wide variety of data sets and data terminals. Eight independent channels are contained on a single board; each is independently programmable to provide the desired channel characteristics.

Sixteen interrupt lines, two for each channel, are provided for communication channel activity sensing.

Functional Description

Channel control is exercised using standard Series/80 instrucitons and a Universal Synchronous/Asynchronous Receiver Transmitter (USART) circuit for each channel.

Channels are double buffered for full duplex transmission and contain data set control to and from modems. Character framing and transmission mode parameters are controlled by programmable features and BERG™ jumpers.

Transmission Characteristics

- Asynchronous
  - — 5-, 6-, 7- or 8-bit characters
  - — Break character generation
  - — 1, 1½, or 2 stop bits
  - — False start bit detect
  - — Odd, even, or no parity
  - — Baud rate of 50 to 19.2K
  - — Ring detect

- Synchronous
  - — 5-, 6-, 7- or 8-bit characters
  - — Automatic SYNC character insertion
  - — SYNC search
  - — Baud rate of 50 to 19.2K
  - — External synchronization
  - — Ring detect

Detection is provided for framing, data overrun and data parity errors.

Either standard programmed I/O or memory mapped I/O program control may be employed. Memory mapped I/O permits memory reference instructions to address the channels. Memory mapped I/O uses a block of 64 bytes of memory; the base address of any 64 byte block is selected using switches on the board.

Electronic Industry Association drivers and receivers are used to insure electrical compatibility of channel interfaces.

Interrupts

Sixteen interrupt lines are available, two for each channel, to notify the system CPU when input data is available for transfer (input buffer full), and when data has been transmitted to the serial line (channel output buffer empty). The 16 interrupt lines are individually maskable under program control, allowing a high degree of channel control flexibility. The interrupts may be OR tied or individually sensed, depending on the CPU used or the mehtod of application.

Connectors

An optional connector kit is available to alleviate the need for special user cabling. The kit consists of a connector board which receives up to four RS232C connectors. The board is designed so that each of the four connectors may be user switched from either a terminal or a modem interface. A cable is provided to connect the BLC-8538 to the connector board. The connector boards may be mounted on the back of a rack mounted computer using a special RMC back panel or on a 19 inch rack using the optional RETMA panel.

Specifications

Channels — 8

Mode — Full duplex

Control — Independent channel

Standard Baud Rates —

50	1800
75	2000
110	2400
134.5	3600
150	4800
300	7200
600	9600
1200	19200

Maximum Baud Rate — 800 KHz

Baud Rate Clock — 5.068 MHz

Baud Rate Synchronization — Internal or external

Interface Standard — RS232C

Interface Signals — Carrier Detect
Clear to Send
Data Set Ready
Data Terminal Ready
Request to Send
Receive Clock
Transmit Clock
Transmit Data
Receive Data
Ring Indicator

System Bus Interface — Data, address and command signals are TRI-STATE™ compatible

Connectors

System Bus — 86 contact double-sided card cage edge connector on 0.156 inch centers

Serial Channel — Two 50 contact double-sided edge connectors on 0.1 inch centers

Recommended mating connector:
3M 3415-0001
AMP 2-86792-3

Power — +5V, 2.9A
+12V, 0.25A
−12V, 0.23A

Environmental — Temperature 0° to 55°C
Humidity 0 to 90% non-condensing

Physical —

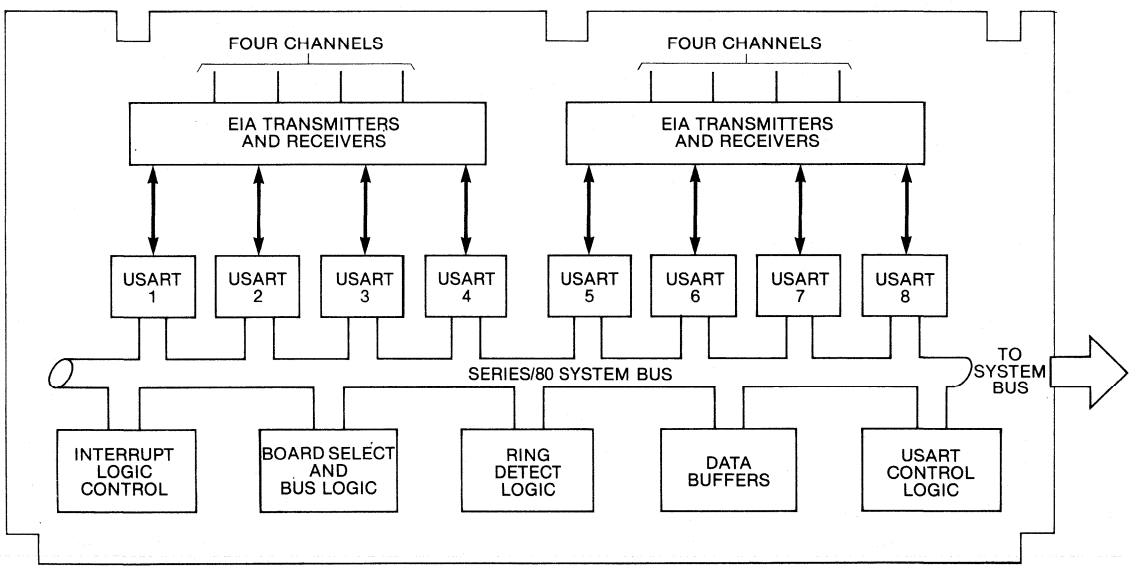
Height	7.05 in.	(17.91 cm)
Width	12.00 in.	(30.48 cm)
Depth	0.50 in.	(1.27 cm)
Weight	12 oz.	(340.2 g)

Order Information

BLC-8538	Eight Channel Communications Expansion Board
BLC-8958	RMC Communications Line Connector Kit (6 in.)
BLC-8958-1	RETMA Communications Line Connector Kit (15 ft.)
RMC-A002	RMC Communications Back Panel
AEE-001	RETMA Communications Termination Panel

Documentation

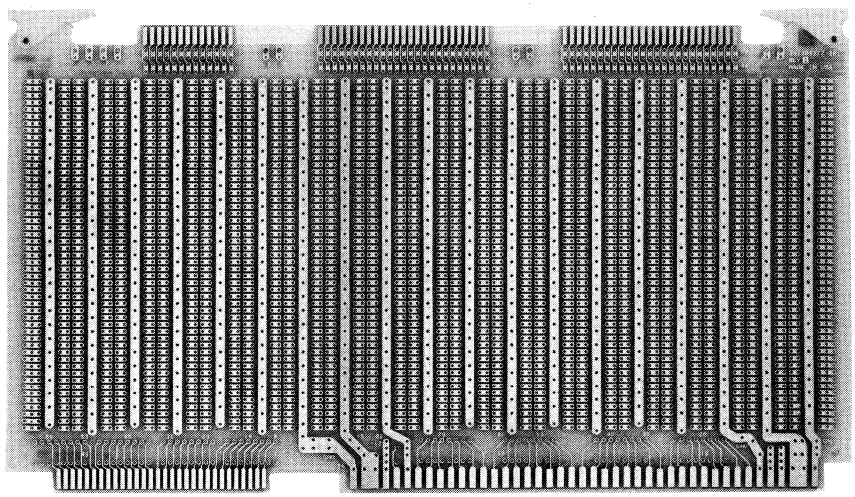
420305528-001	Eight Channel Communications Expansion Board Hardware Reference Manual



BLC-8538 Diagram

National Semiconductor

BLC-8905 and BLC-905 Universal Prototyping Boards



- **Capacity for 108 16-pin DIP's**
- **Choice of Top Edge Connectors**
- **Permits Easier User Construction of Custom Circuitry for BLC/SBC Systems**

Product Overview

The BLC-8905 and BLC-905 provide ready-made, low-cost solutions to the problem of mounting custom circuits in a BLC/SBC computer system. These prototyping boards are designed to accept up to 108 16-pin sockets, integrated circuits, or an equivalent mix of 14, 16, 18, 22, 24, 28, and 40 pin configurations.

Functional Description

The BLC-905 contains one 100 contact top edge connector, and the standard P1 and P2 edge connectors for insertion into a BLC/SBC-604 or -614 card cage backplane.

The BLC-8905 contains two 50 contact connectors and one 26 contact top edge connector.

Specifications

Connectors (BLC-8905)

System Bus — 86 contact double-sided card cage edge connector on 0.156 inch centers

Parallel I/O — 50 contact double-sided edge connector on 0.10 inch centers

Recommended mating connector:
3M 3415-0001 or equivalent

Serial I/O — 26 contact double-sided edge connector on 0.10 inch centers

Recommended mating connector:
3M 3462-0001 CRIMP or equivalent

Connectors (BLC-905)

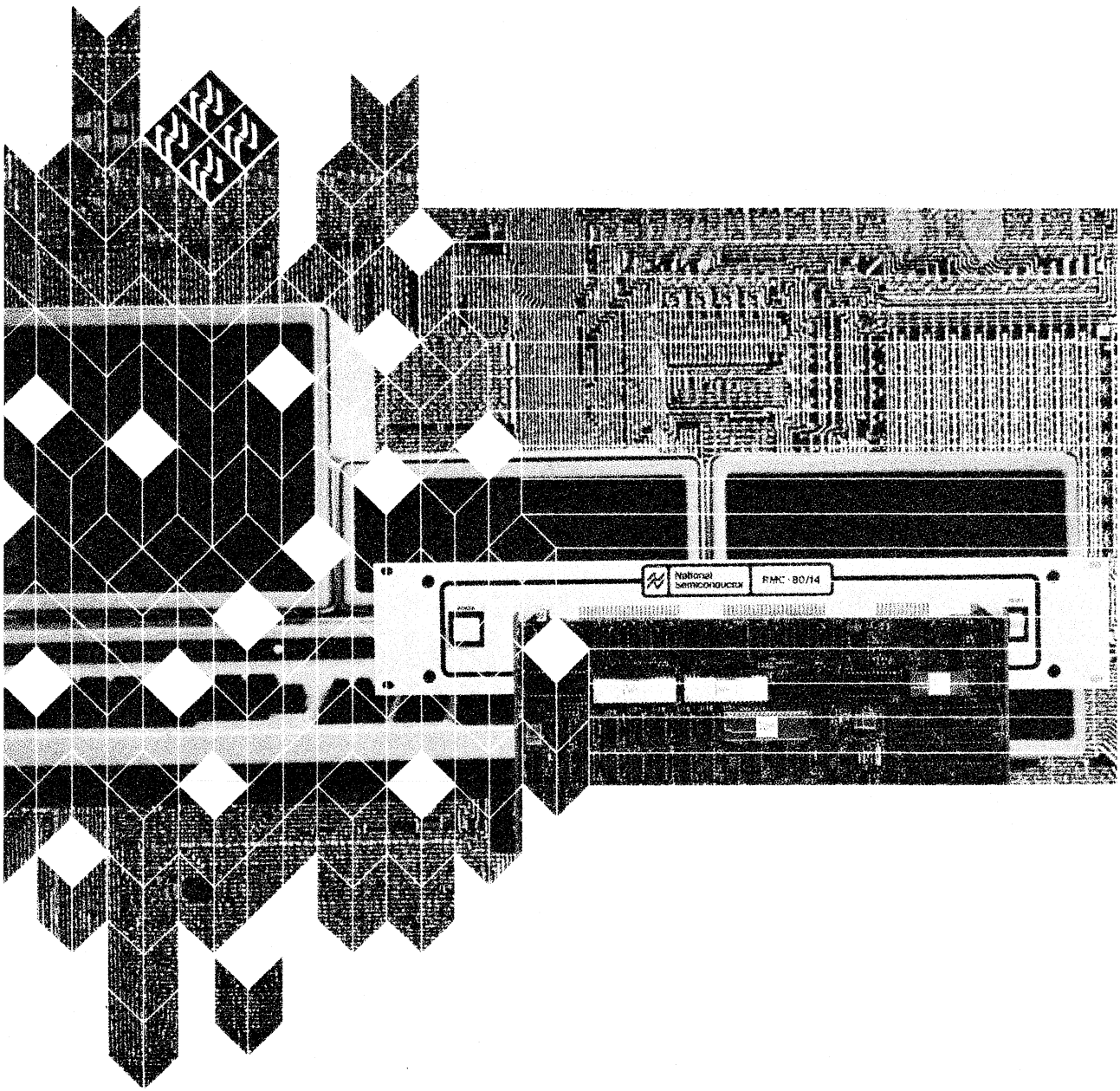
System Bus —	86 contact double-sided card cage edge connector on 0.156 inch centers
Top Edge —	100 contact double-sided edge connector on 0.10 inch centers Recommended mating connector: CDC VPB04B50E00A1E
Environmental	Temperature 0° to 55°C Humidity 0 to 90% non-condensing

Physical			
	Height	6.75 in.	(17.15 cm)
	Width	12.00 in.	(30.48 cm)
	Depth	0.50 in.	(1.27 cm)
	Weight	5 oz.	(141.75 g)

Order Information

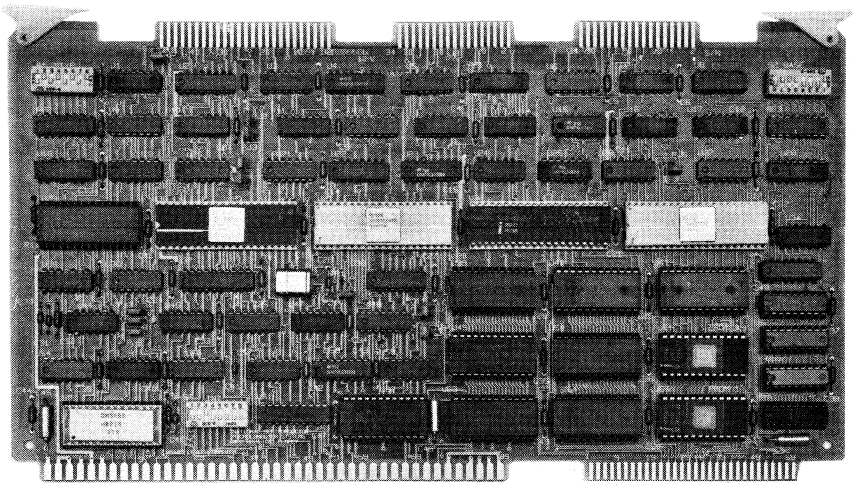
BLC-905	Universal Prototyping Board with one 100 contact top edge connector
BLC-8905	Universal Prototyping Board with two 50 contact and one 26 contact top edge connectors

Section 6
Peripheral Controllers



National Semiconductor

BLC-8201 and BLC-8221 Floppy Disc Controllers



- **Intelligent Non-Volatile Bulk Storage Controller on a Single Series/80 Board**
- **Designed for User Flexibility**
  - DMA data transfers
  - Multi-master bus control
  - On-board 8080A CPU
  - 4K byte EPROM for custom applications, 1K byte RAM
  - Automatic seek error retry
- **Interfaces to Single Density Standard or Mini Floppy Disc Drives — Single or Dual Side Recording**
- **CRC Integrity Error Checking**
- **Large Capacity Systems**
  - Support up to four disc drives
  - Multiple controllers allowed in a single system
- **GO-NO GO Diagnostic Monitor for Use on System CPU Board**
- **BLC-8201 — Intel SBC-201 Operating Mode but Requires 70% Less Power**

Product Overview

The BLC-8221 and BLC-8201 Floppy Disc Controllers are members of National's Series/80 family of peripheral device intelligent controllers. The controllers interface directly with a variety of standard and mini size floppy disc drives, adding significant data and program storage capacity to an OEM microcomputer system. The BLC-8201 is a single board plug-replacement for the two-board SBC-201.

The BLC-8221 and BLC-8201 incorporate the latest in LSI technology to provide a significant amount of on-board control power while minimizing the component count. This results in 70% less power consumption than an SBC-201 controller.

The controllers are capable of controlling up to four single side or two double side recording floppy disc drives. The disc drive heads are automatically unloaded by the controller if there has been no data change in six revolutions. This prevents unnecessary wear of the disc media.

Data integrity is assured by cyclic redundancy checking (CRC) data validation.

Functional Description

The BLC-8221 and BLC-8201 single density floppy disc controllers perform any of seven different operations under direction of the system CPU. The operations are: recalibrate, seek, format, track, write data, write deleted data, read data, and verify CRC. The system CPU communicates with the controller via programmed I/O and Direct Memory Access (DMA) for commands and data. Once a command is set up and initiated by the CPU, the controller completes the operation without further CPU intervention. The BLC-8201 is designed to communicate with Intel's MDS-DOS system. Standard communications between the system CPU and the controller proceed as follows:

The system CPU prepares a 10 (BLC-8201) or 12 (BLC-8221) byte Input/Output Parameter Block (IOPB) in main memory. The IOPB contains complete instructions to specify the disc operation. (See Figure 1.) The address is main memory for data transfer, read or write disc, interrupt when done, etc., are all determined by the IOPB. After building the IOPB in memory, the CPU passes the address of the IOPB using two output instructions. The controller sets its busy status and reads the IOPB from main memory using DMA transfer. When the operation defined in the IOPB is complete, the busy flag is reset and an interrupt is generated, if specified by the IOPB instructions. If the operation specified by the IOPB is a data transfer, data is transferred to and from main memory by DMA. With the BLC-8221 the IOPB may specify buffered data transfers, using the controller's RAM, or unbuffered data transfers. BLC-8201 data transfers are always unbuffered.

Controller logical structure permits the IOPB to define command chaining. In this way, the system CPU can specify any desired sequence of disc operations. The controller completes chained operations autonomously.

Errors are recorded in status bits for condition sensing and recovery. Seek errors are recorded after 3 retries. The IOPB may be used to signify a system interrupt from the controller when an error condition is encountered.

	Content							
	7	6	5	4	3	2	1	0
Byte 1	Channel Word							
2	Floppy Disc Instruction							
3	Number of Records							
4	Track Address							
5	Sector Address							
6	Main Memory Buffer Address (Low Order Bits)							
7	Main Memory Buffer Address (High Order Bits)							
8	Block Number							
9	Next IOPB Address (Low Order Bits)*							
10	Next IOPB Address (High Order Bits)*							

*Chained operations.

a. BLC-8201 — IOPB Format

	Content							
	7	6	5	4	3	2	1	0
Byte 1	Disc Number		Interrupt Control		IOPB Length	Disc Command		
2	Number of Sectors							
3	Track Number							
4	Sector Number							
5	Buffer Address Low							
6	Buffer Address High							
7	Sector Length							
8	Data Mark		Retry Level		IBM Format	Buffer Start		
9	Err Flag	Not Used	Block Tag					
10	Not Used		Disc Side	Not Used		Buf or Unbuf	DD or SD	Cmd Chain
11	Next IOPB Address Low							
12	Next IOPB Address High							

b. BLC-8221 — IOPB Format

Figure 1. IOPB Format

Specifications

Data Word Length —	8 bits parallel
Memory Address Range —	64K bytes
Data Transfer Modes —	DMA Programmed I/O
Data Transfer Rate —	Up to 78 KB per second
Data Buffer —	1K bytes
CPU —	INS8080A
Disc Controller —	INS1771
Disc Drive Capability —	4 single sided or 2 dual sided

Disc Drive Characteristics —

Disc Drive Compatibility	Shugart Model 800 (BLC-8221 and 8201) or 400 Series (BLC-8221) or equivalent
Sector Type	Soft sectored
Recording	Single density
Tracks	77 for 8 inch standard 35 for 5 1/8 inch mini
Sectors per Track for 128 Byte Sector	26 for 8 inch standard 18 for 5 1/8 inch mini
Bytes per Sector	16 to 512 (128 for BLC-8201)
Formatted Storage per Surface	256K bytes for 8 inch standard 80K bytes for 5 1/8 inch mini

System Bus Interface —	Data, address and command signals are TRI-STATE™ TTL compatible

Connectors —

System Bus	86 contact double-sided card cage edge connector on 0.156 inch centers
Auxiliary	One 60 contact double-sided edge connector on 0.1 inch centers
Standard Size Disc Drives	Two 34 contact double-sided edge connectors on 0.1 inch centers Recommended mating connector: 3M "Scotchflex" 3463-0001
Mini Size Disc Drives	One 50 contact double-sided edge connector on 0.1 inch centers Recommended mating connector: 3M "Scotchflex" 3415-0001
Power —	+5V, 2.0 A −5V, 0.25 A +12V, 0.06 A
Environmental —	Temperature 0° to 55°C Humidity 0 to 90% non-condensing

Physical —

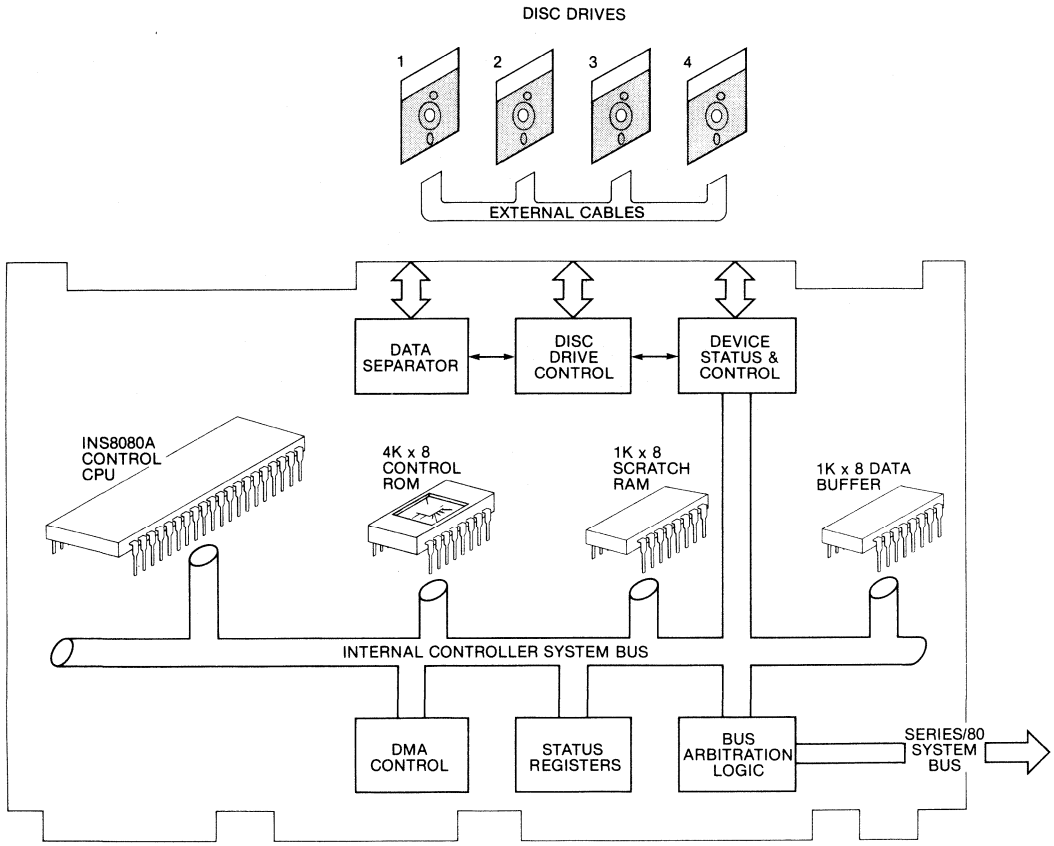
Height	6.75 in.	(17.15 cm)
Width	12.00 in.	(30.48 cm)
Depth	0.50 in.	(1.27 cm)
Weight	14 oz.	(396.9 g)

Order Information

BLC-8201	Floppy Disc Controller with MDS-DOS Emulation Mode
BLC-8221	Floppy Disc Controller

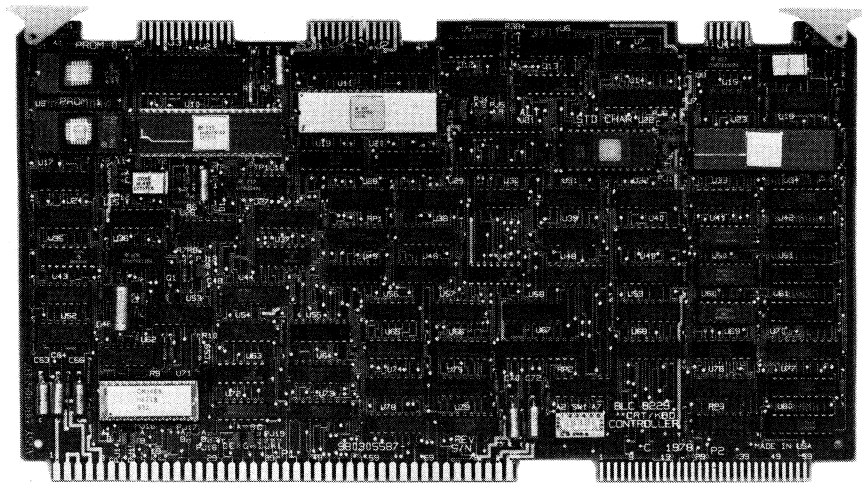
Documentation

420305586-001	BLC-8221/BLC-8201 Floppy Disc Controller Hardware Reference Manual



BLC-8201 and BLC-8221 Diagram

BLC-8228 and BLC-8229 Video Monitor/Keyboard Controllers



- **Intelligent Controller on a Single Series/80 Board**
- **Designed for User Flexibility**
  - DMA transfers for rapid screen update
  - Interrupt control
  - On-board 8080A CPU and control ROM
  - 1K byte scratch pad RAM
  - Complete editing function, control logic and scrolling
  - EPROM sockets for user-defined alternate character set
  - Programmable display attributes: blink, blank, inverse video and alternate character set
  - Full software cursor control
  - 3 wire video output
- **On-Board Video Refresh Memory**
- **Full 128 ASCII Character Set**
- **24 Line by 80 Character Display Array**
- **Selection of Display Matrix**
  - 5 by 7 — BLC-8228
  - 7 by 9 — BLC-8229
- **Compatible with All Series/80 Boards and Card Cages**

Product Overview

The Video Monitor/Keyboard Controller is a member of National's Series/80 family of peripheral device intelligent controllers. It is fully compatible with all National Series/80 boards and plugs directly into any Series/80 card cage backplane or system. The controller is available in two models, BLC-8228 and BLC-8229. The BLC-8228 provides a 5x7 dot matrix character while the BLC-8229 provides a 7x9 dot matrix character.

All that is required to make the BLC-8228 or BLC-8229 an intelligent CRT terminal is the addition of a standard ASCII encoded keyboard and a low cost monitor. The controller provides a display array of 24 lines by 80 characters. The character generator consists of a 128 upper and lower case ASCII character set. The controller can also accommodate a user-supplied custom alternate character set which may be software selected on a character-by-character basis.

Full software cursor control (up, down, left, right, home, set, indirect, sense) and screen formatting codes are included to yield a very powerful screen editor. Although on-board firmware provides numerous special editor functions, the user may implement custom editing and formatting functions by writing his own firmware. (See Table I for standard functions.)

Each character is assigned one of four attributes: blink, blank, inverse or alternate character. Scrolling is software selectable for each display line. In this way selected lines can be excluded from scrolling. Non-displayable ASCII control codes (e.g., ACK, EOT, etc.) may be displayed on the monitor and occupy only one display character position. An on-board tone generator is available for connection to an external speaker. The cursor may be represented as block inverse or underscore (blinking or non-blinking).

Functional Description

The BLC-8228 and BLC-8229 contain an on-board 8080A CPU with up to 4 KB of space for instruction ROM/PROM (2K bytes using MM2708 PROM or 4K bytes using MM2716 EPROM), a 1K byte scratch pad RAM, 2K character buffer and 2K x 4 bits buffer RAM for character attribute codes, 2K byte refresh RAM, a CRT controller chip, and 2 sockets for standard and alternate character generators.

Characters generated by the user's encoded keyboard enter the controller as an 8-bit parallel transfer under interrupt control. The controller transmits the character to the host CPU, which then processes it and transmits it back for display.

Communication between the host CPU and the controller is accomplished in byte parallel via the main system data bus. An 8-bit status register is also available to the host CPU via the main system data bus. Character data can be moved between the controller's RAM buffer and main system memory in DMA mode to provide high speed data transmission.

One of two character generator PROM's (standard or alternate) is enabled according to the state of the controller font bit.

The controller provides 3 host maskable interrupts, CRT Ready, Keyboard Ready and ERROR, to the host CPU. Each of these may be jumpered to any of 9 main bus interrupt lines. The interrupt information is also available to the system by reading the status register contents.

Video output consists of separate horizontal sync, vertical sync and video out signals. STEP-SCAN™ is a jumper selectable option on the BLC-8229 which produces a screen display with more than one line of space between rows and no interleaving blank lines between rows and columns. STEP-SCAN is typically used in normal character applications where the extra space produces an exceptionally clear and easy-to-read 7x9 matrix display.

Controller integrity is assured by execution of on-board tests which are automatically activated upon receipt of a system reset. The validation testing exercises the controller RAM, PROM and I/O display ports.

Table I. Editor Functions and Software Switches (On/Off)

CURSOR	Set Cursor Set Cursor Indirect Set Cursor On Set Cursor Off Sense Cursor Move Cursor Right Move Cursor Left Move Cursor Up Move Cursor Down Move Cursor Home
LINE	Enter Insert Line Insert Line Exit Insert Line Delete Line Erase to End of Line Auto Carriage Return On/Off (80 column)
CHARACTER	Enter Insert Character Insert Character Delete Character Destructive Backspace On/Off Upper Case On/Off
TAB	Set Tab Clear Tab Clear All Tabs Back Tab Destructive Back Tab On/Off
DMA	Enter DMA Mode Enter DMA With Count Exit DMA Mode Privileged Mode On/Off
SCROLL	Roll Up Roll Down Next Page Erase to End of Screen Fix Line Unfix Line Unfix All Lines
ATTRIBUTES	Set Attributes Write Attributes Dump Attribute Memory
SCREEN	Dump Screen Memory Load Screen Memory
MISCELLANEOUS	Write Character Reset Call Subroutine Set LED Set/Reset Software Switches Clear FIFO Buffer

7	6	5	4	3	2	1	0
Keybd Ready	CRT Ready	Error Flag					
			Error Code				

a. Status Register

7	6	5	4	3	2	1	0
Keybd Ready Intrpt Enable	CRT Ready Intrpt Enable	No Error Intrpt Enable	Not Used	Not Used	Not Used	Not Used	Not Used

b. Interrupt Mask Register

7	6	5	4	3	2	1	0
Char/ Control Code							
				Data			

c. Data Word

Figure 1. Status, Interrupt and Data Format

Specifications

Data Transfer Mode —	DMA or Programmed I/O
DMA Transfer Rate —	Up to 78K bytes per second
CPU —	INS8080A
Video Monitor Controller —	DP8350 (5x7) DP8353 (7x9)
Scratch Pad Buffer —	1Kx8-bit RAM
Attribute Buffer —	2Kx4-bit RAM
Instruction ROM —	2Kx8-bit (standard firmware MM2708) 4Kx8-bit sockets (MM2716 as a user-implemented option)
Character Generator —	Standard 128 character upper/lower case ASCII May also contain user-implemented character set (INS2708 or 2716)
Keyboard Input Port —	5 character FIFO buffered 8 data lines and 1 strobe from keyboard
Audio Signal Generator —	1800 Hz for 0.15 seconds
Special Function Register —	4 bits wide for external LED indicators or custom flags
Display —	24 rows by 80 columns 5x7 dot matrix (BLC-8228) 7x9 dot matrix (BLC-8229) Individual character attributes: blink (2 Hz) blank inverse video alternate character set Cursor types (jumper selectable): block inverse video underscore (BLC-8229 only) none Frequency 50 or 60 Hz
Address —	Switch select four of 16 available
Bus Interface —	
System	Address, data and command signals are TRI-STATE™ TTL compatible
Video Monitor Interface	Horizontal and vertical sync are TTL compatible Video Out: Low — 0.2V Med — 1.6V (inverse characters) High — 2.2V Frequency: 15.9 KHz (BLC-8228) 18.0 KHz (BLC-8229)
Connectors —	
System Bus	86 contact double-sided card cage edge connector on 0.156 inch centers Recommended mating connector: CDC VPB01E43A00A1 or equivalent
Keyboard	26 contact double-sided edge connector on 0.1 inch centers Recommended mating connector: 3M 3462-0001, TI H3/2113 or equivalent
Video Monitor	12 contact double-sided edge connector on 0.1 inch centers Recommended mating connector: AMP 2-583717-1 or equivalent

Power — +5V, 4.90 A
−5V, 0.91 A
+12V, 0.22 A
−12V, 0.30 A

Environmental — Temperature 0° to 55°C
Humidity 0 to 90%
non-condensing

Physical —

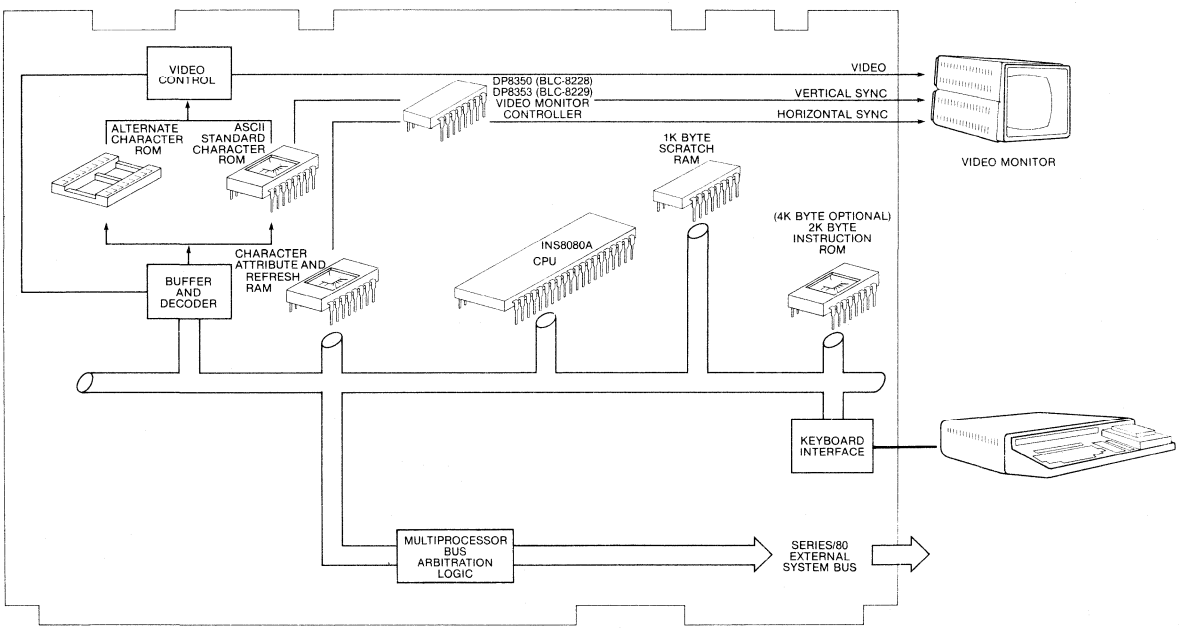
Height	6.75 in.	(17.15 cm)
Width	12.00 in.	(30.48 cm)
Depth	0.50 in.	(1.27 cm)
Weight	14 oz.	(396.9 g)

Order Information

BLC-8228	Video Monitor/Keyboard Controller with 5x7 dot matrix character generator
BLC-8229	Video Monitor/Keyboard Controller with 7x9 dot matrix character generator

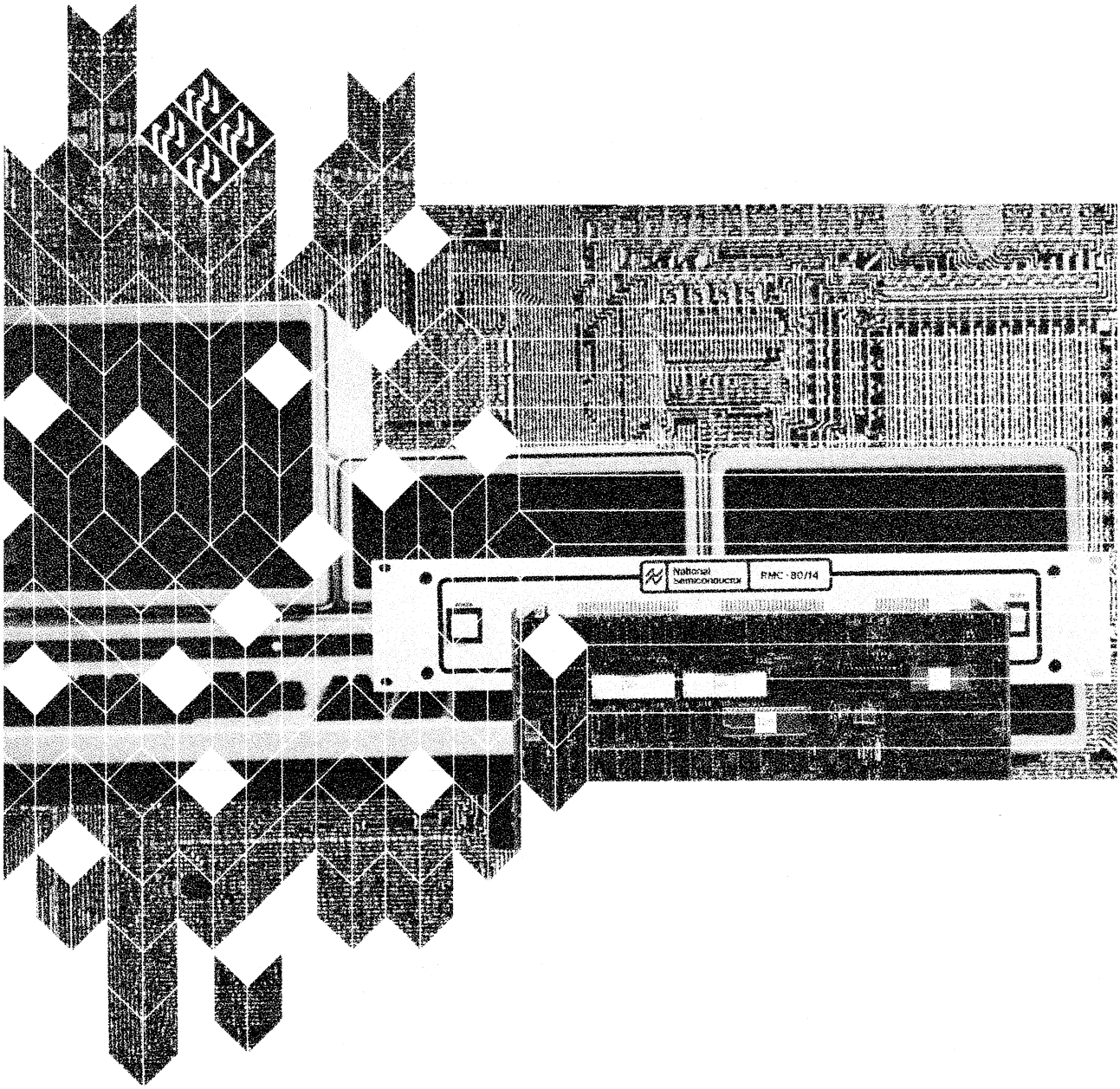
Documentation

420305587-001	CRT/Keyboard Controller Board Hardware Reference Manual



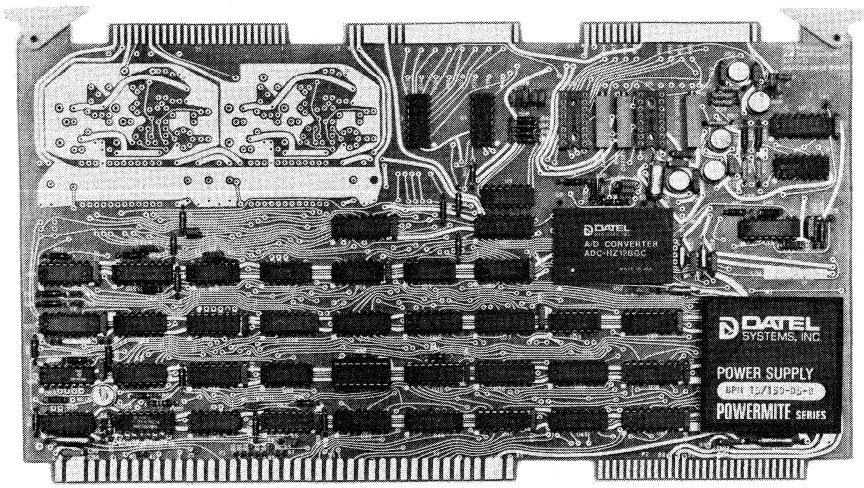
BLC-8228 and BLC-8229 Diagram

Section 7
Analog Input/Output Boards



National Semiconductor

BLC-711
Analog Input Board



- **Application Flexibility**
  - 16 single-ended/8 differential channels
  - Expandable to 32 single-ended/16 differential channels
  - Voltage or current mode inputs
  - Sequential, random and single channel scan modes
- **50 KHz Sample Rate Permits Use in Wide Range of Applications**
- **12-bit Resolution with 0.05% Overall Accuracy for Precise Measurements**
- **On-board Pacer Clock or External Synchronization of Sampling for System Flexibility**
- **Programmable Gain Amplifier Accommodates Wide Range of Systems**
- **Plug-replacement for SBC-711**

Product Overview

The BLC-711 Analog Input Board extends the Series/80 family of microcomputer products into a wide variety of instrumentation and process control applications.

The BLC-711 provides multiple analog input capability. Analog input functions allow data sampling at a rate of 50,000 samples per second and storage of equivalent digital values for subsequent processing. The BLC-711 is equipped with sample and hold circuitry, and accuracy of conversion is assured by holding the input sample constant until conversion is completed. Analog inputs may be sampled in a random, sequential, or single channel repetitive mode.

The board contains a high resolution 12-bit analog converter, 16 single-ended or 8 differential input channels, programmable gain amplifier, and the sample and hold function. The analog input capacity is expandable to 32 single-ended or 16 differential channels.

The BLC-711 is a plug-compatible replacement for Intel's SBC-711.

Functional Description

Standard Series/80 instructions control analog input channels. Memory mapped I/O simplifies the transfer of data with simple memory reference instructions to predefined memory locations.

With memory mapped I/O, a segment of 16 contiguous addresses is predefined and set on the board. These addresses may be on any even 16 byte boundary within the 64K bytes of available address space. If these addresses overlay system memory addresses, memory inhibit logic prevents address contention for memory mapped I/O addresses.

Analog Input

Analog to digital (A/D) conversion is initiated by a Write command to the Multiplexer Address Register (MAR). The bit pattern of the MAR specifies the gain and the specific channel to be converted. The Command Register (CR) is then loaded with a bit pattern that enables conversion and the desired interrupts. Bits in the Command Register also specify pacer clock/external trigger, the board busy bit, and enabling sequential scan.

If the sequential scan feature is enabled, input channels will be sequentially converted until the channel address in the Last Channel Register (LCR) is reached.

Data sent to the Command Register can be read back by issuing a Read command to the Status Register (SR). In addition to verifying the last command word sent to the Command Register, the status also signifies that conversion has been completed or that the last channel has been reached.

After analog conversion is complete, the corresponding digital data value is read from the converter register. The first byte contains the low order 4 bits (bits 0 to 3) of the digital representation; the second byte contains the 8 high order bits (bits 4 to 11).

The selected analog input is applied to the A/D converter through a software controlled programmable gain amplifier which provides gains of X1, X2, X4, or X8, and a sample and hold amplifier. With the A/D converter jumper selected for +5V, +10V, ±5V, or ±10V full scale input voltages, the gain amplifier permits sampling of analog input voltages as shown in Table I.

Table I. Programmable Gain Full Scale Values

Gain Selected	Voltage Range Selection			
	+5V	+10V	±5V	±10V
X1	+5V	+10V	±5V	±10V
X2	+2.5V	+5V	±2.5V	±5V
X4	+1.25V	+2.5V	±1.25V	±2.5V
X8	+0.625V	+1.25V	±0.625V	±1.25V

Sampling is controlled in one of three ways: by program instruction (writing the multiplexer address to an analog input channel), by an internal sample timer (pacer clock), or by external event synchronization (external trigger). The pacer clock may be jumper configured to provide timing intervals from 975 microseconds to 1 second.

Interrupts to the system CPU may be generated upon completion of either a channel sample conversion or a sequential channel scan. This relieves the system CPU of continuous status scanning.

The analog input control parameters are illustrated in Figure 1.

7	6	5	4	3	2	1	0
Gain Select	Gain Select	Not Used	2^4	2^3	2^2	2^1	2^0

Channel Select

Gain	Bit 7	Bit 6
X1	0	0
X2	0	1
X4	1	0
X8	1	1

a. Multiplexer Address and Gain Format

7	6	5	4	3	2	1	0
Not Used	Not Used	Not Used	2^4	2^3	2^2	2^1	2^0

Last Channel Address

b. Last Channel Sampled Address Format

7	6	5	4	3	2	1	0
Not Used	Not Used	End of Conv. Intrpt	End of Scan Intrpt	Clear Busy	Exit Trig Enable	Auto Incr Enable	Start/ Stop

c. Command Register Byte Format

7	6	5	4	3	2	1	0
Conv. Done	Scan Done	End of Conv. Intrpt	End of Scan Intrpt	Busy	Exit Trig Enabl	Auto Incr Enabl	Start/ Stop

d. Status Register Byte Format

7	6	5	4	3	2	1	0
Not Used	Not Used	Clear End of Conv. Intrpt	Clear End of Scan Intrpt	Clear Pacer Clock	Not Used	Not Used	Not Used

e. Clear Interrupts Format

Address	Write Command Description
Base + 0	Load Command Register (CR)
Base + 1	Load Multiplexer Address Register (MAR)
Base + 2	Load Last Channel Register (LCR)
Base + 3	Clear Interrupts

Address	Read Command Description
Base + 0	Read Status Register (SR)
Base + 1	Read Multiplexer Address Register (MAR)
Base + 4	Read LS Byte, A/D (ADCR)
Base + 5	Read MS Byte, A/D (ADCR)

f. Memory Mapped Addressing

Figure 1. Analog Control Parameters

DC to DC Converter

The board contains a DC to DC converter to convert the +5 VDC power input to the ±15 VDC required by analog circuitry. The converter input may be changed to permit the direct connection of external regulated voltages. This option is implemented with on-board jumpers and connection of the voltage via the auxiliary backplane connector.

Diagnostic Test

A diagnostic test program is included with the BLC-711 to allow testing the analog circuits.

Specifications

Scan Mode —	Sequential; Random; Single Channel Repeat
Channels —	16 single-ended or 8 differential
Channel Resolution —	11 bits plus sign, 2-s complement bipolar 12 bits, unipolar or offset binary
Full Scale Range Volts —	0 to +0.625; +1.25; +2.5; +5 0 to +1.25; +2.5; +5; +10 ±0.625; ±1.25; ±2.5; ±5 ±1.25; ±2.5; ±5; ±10
Programmable Gain —	X1, X2, X4, X8
Sample and Hold —	
Aperture Time	Less than 100 nanoseconds
Uncertainty Time	20 nanoseconds
Acquisition	8 microseconds
Throughput Rate —	24 KHz
A/D Conversion Speed —	50 KHz
Overall Accuracy — (25 °C)	Less than 0.05% FSR ± ½ LSB (Gain 1X) Less than 0.07% FSR ± ½ LSB (Gain 2X, 4X, 8X) [Includes 3 sigma noise, linearity, offset gain and dynamic response errors]
Input Impedance —	680 ohms (power off) Greater than 100 megaohms (power on)
Input Current —	0 to 20 ma (with 250 ohm user installed resistors)
Common Mode —	
Voltage	±10.24 V maximum (signal and common mode)
Rejection	−60 db (differential input) at source impedance: Balanced — less than 5000 ohms Unbalanced — less than 1000 ohms
Crosstalk —	−86 db at 10 KHz
Overvoltage Protect —	±35 VDC, AC peak
Temperature Coefficient —	Less than 0.003% FSR/ °C
Monotonicity —	Guaranteed over the operating temperature range
External Trigger —	±4 V for 200 ns (min) with ≤50 ns rise time
Pacer Clock —	Crystal controlled, 0.05% accuracy Divider range $\frac{1000}{2^n}$ ms (n = 0 through 10)
System Bus Interface —	Data, address and command signals are TRI-STATE™ TTL compatible
Connectors —	
System Bus	86 contact double-sided card cage edge connector on 0.156 inch centers
Analog	One 50 contact input double-sided edge connector on 0.1 inch centers Recommended mating connectors: 3M 3415-000, TIH312125 or equivalent One 60 contact auxiliary double-sided edge connector on 0.1 inch centers Recommended mating connectors: CDC VPB01B30A00A2 AMP PES-14559 TIH 311130 One 50 contact input expansion double-sided edge connector on 0.1 inch centers Recommended mating connectors: 3M 3415-000, TIH 312113 or equivalent

Power — +5V, 2.3A
If Auxiliary Power is used:
±15VDC ±5%, 150ma

Environmental — Temperature 0° to 55°C
Humidity 0 to 90%
non-condensing

Physical —

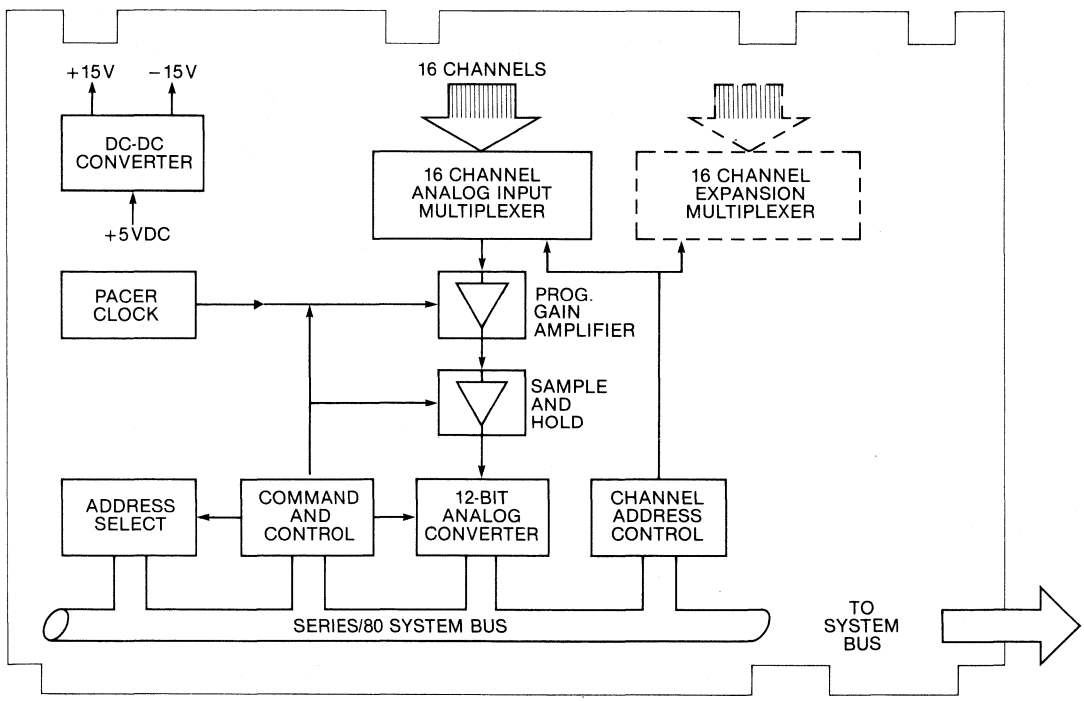
Height	6.75 in.	(17.15 cm)
Width	12.00 in.	(30.48 cm)
Depth	0.50 in.	(1.27 cm)
Weight	20 oz.	(567 g)

Order Information

BLC-711	Analog Input Board Includes 16 single-ended or 8 differential analog input channels, manual and diagnostic test program in paper tape media

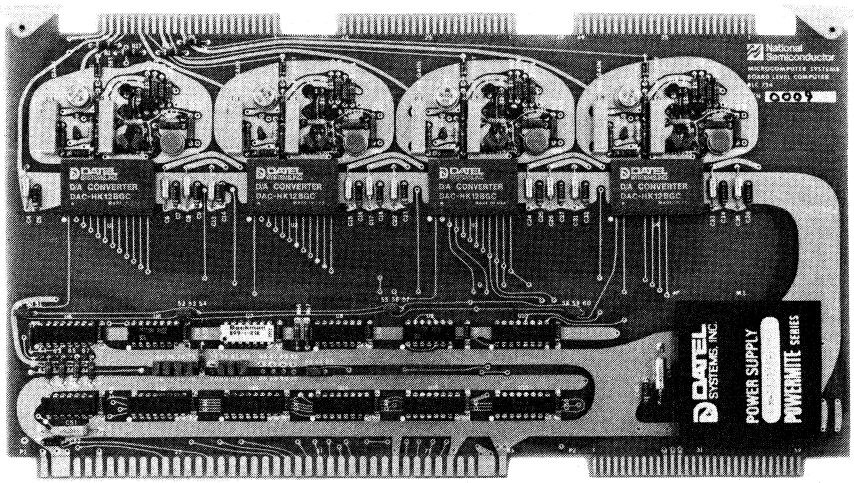
Documentation

420305649-001	BLC-711 and BLC-732 Analog Input and Combination Input/Output Board Hardware Reference Manual



BLC-711 Diagram

BLC-724
Analog Output Board



- **Application Flexibility**
  - Four independent channels
  - Unipolar and bipolar operation
  - Voltage and current mode outputs
- **Fast 3 Microsecond Settling Time**
- **12-bit Resolution with 0.05% Accuracy for High Overall Accuracy**
- **Plug-replacement for SBC-724**

Product Overview

The BLC-724 Analog Output Board extends the Series/80 family of microcomputer products into a wide variety of instrumentation, control and analog display applications.

Compatible with the Series/80 system bus, the board provides the logic functions necessary to convert digital data to analog output signals. Four independently controlled channels are provided, each with 12-bit resolution.

Analog outputs may be unipolar or bipolar, thus providing application flexibility. Channel output is from 0 to ±10 volts or may be employed in a 4 to 20 milliamp current loop mode.

The BLC-724 is a plug-compatible replacement for the Intel SBC-724.

Functional Description

Standard Series/80 instructions control analog output. Memory mapped I/O simplifies the programming task by permitting the transfer of output data with simple memory reference instructions to predefined memory locations.

With memory mapped I/O a segment of 8 contiguous addresses is predefined and set on the board. These addresses may be on any 8 byte boundary within the 64K bytes of available address space. Analog output starts when the most significant byte (second byte) of the Write command is transferred to the digital to analog channel converter. The control parameter configuration is illustrated in Figure 1. Memory inhibit logic prevents address contention for memory mapped I/O addresses.

7	6	5	4	3	2	1	0
Data 11 (MSB)	Data 10	Data 9	Data 8	Data 7	Data 6	Data 5	Data 4

Second Byte (MS Byte)

7	6	5	4	3	2	1	0
Data 3	Data 2	Data 1	Data 0 (LSB)	0	0	0	0

First Byte (LS Byte)

Address	Write Command Function	Channel
Base + 0	Load LS Byte	0
Base + 1	Load MS Byte	0
Base + 2	Load LS Byte	1
Base + 3	Load MS Byte	1
Base + 4	Load LS Byte	2
Base + 5	Load MS Byte	2
Base + 6	Load LS Byte	3
Base + 7	Load MS Byte	3

Figure 1. Analog Output Control Parameters

DC to DC Converter

The board contains a DC to DC converter to convert the +5 VDC power input to the ±15 VDC required by the analog generating circuitry. The converter input may be changed to permit the direct connection of external regulated voltages. This option is implemented with on-board jumpers and connection of the voltage via the auxiliary backplane connector.

Diagnostic Test

A diagnostic test program is included with the BLC-724 to allow testing and calibration of the analog output channels. Calibration is recommended when a channel range jumper is set.

Specifications

General

Number of Channels — 4 non-isolated

Channel Resolution — 12 bits including sign

Slew Rate — 10 volts per microsecond (no external capacitance)

Settling Time — 3 microseconds to ½ LSB (5 volt step change)

Accuracy — 0.05% FSR at 25°C (includes linearity and noise)

Monotonicity — Guaranteed over operating temperature range

Voltage Mode Output Characteristics

Full Scale Range (Jumper Select) — 0 to +5V, 0 to +10V, ±5V, ±10V

Output Current — ±5ma at ±10V

Output Impedance — 0.05 ohms

Output Capacitance — 1000pf maximum

Current Mode Output Characteristics

Full Scale Range — 4 to 20ma current loop, unipolar (requires external loop voltage of 15 to 30VDC)

Load Impedance — 500 ohms maximum

Other

System Bus Interface — Data, address and command signals are TRI-STATE™ TTL compatible

Connectors —

System Bus — 86 contact double-sided card cage edge connector on 0.156 inch centers

Auxiliary — One 60 contact double-sided edge connector on 0.1 inch centers

Recommended mating connectors:
CDC VPB01B30A002
AMP PES-14559
TIH 31110

Analog Output — One 50 contact double-sided edge connector on 0.1 inch centers

Recommended mating connector:
3M 3415-000,
TIH 312125, or equivalent

Power — +5V, 1.5A

If Auxiliary Power is used:
±15VDC ±5%, 150ma

Environmental — Temperature 0° to 55°C
Humidity 0 to 90%
non-condensing

Physical —

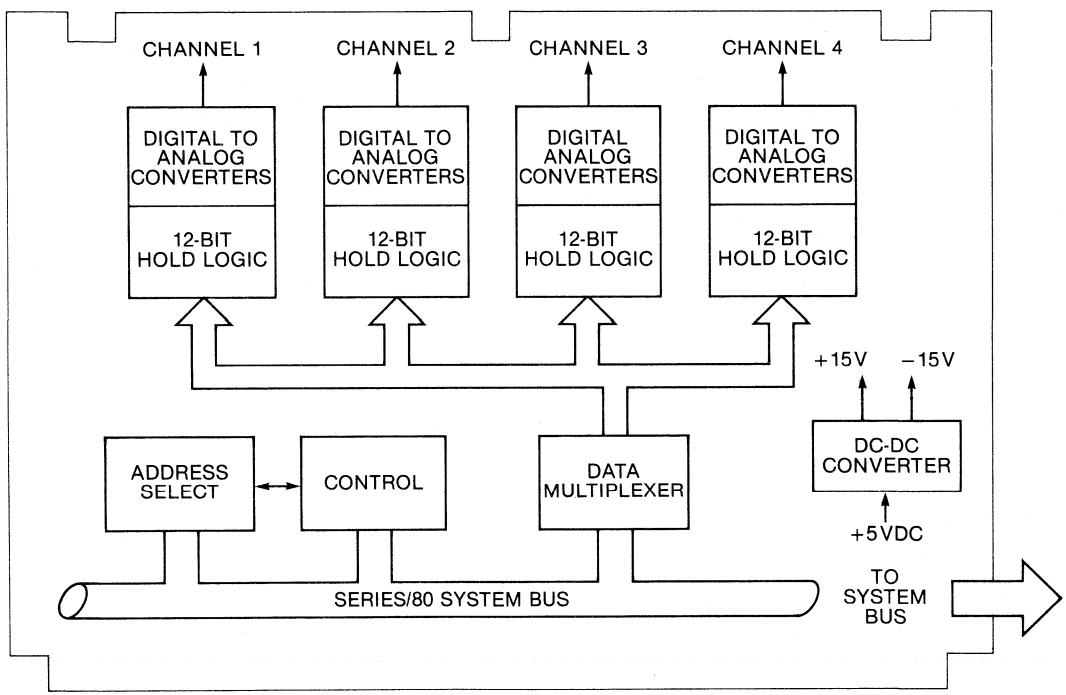
Height	6.75 in.	(17.15 cm)
Width	12.00 in.	(30.48 cm)
Depth	0.50 in.	(1.27 cm)
Weight	18 oz.	(510.3 g)

Order Information

BLC-724	Analog Output Board Includes 4 independent high level analog output channels, manual and diagnostic test program in paper tape media.

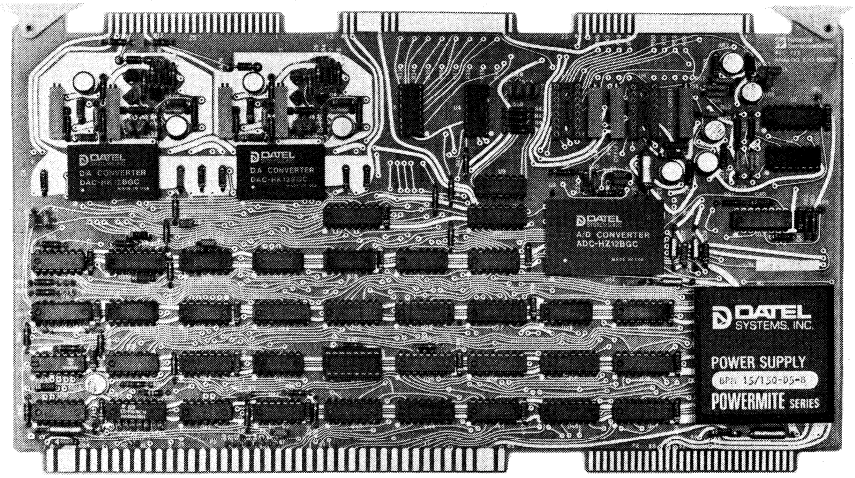
Documentation

420305647-001	BLC-724 Analog Output Board Hardware Reference Manual



BLC-724 Diagram

BLC-732
Combination Analog Input/Output Board



- **Application Flexibility**
  - 16 single-ended/8 differential channels
  - Expandable to 32 single-ended/16 differential channels
  - 2 output channels
  - Unipolar and bipolar operation
  - Voltage and current mode inputs and outputs
  - Sequential, random and single channel scan modes
- **50 KHz Sample Rate Permits Use in Wide Range of Applications**
- **12-bit Resolution with 0.05% Overall Input and 0.05% Output Accuracy for Precise Measurements**
- **On-board Pacer Clock or External Synchronization of Sampling for System Flexibility**
- **Programmable Gain Amplifier Accommodates Wide Range of Systems**
- **Plug-replacement for SBC-732**

Product Overview

The BLC-732 Combination Analog Input/Output Board extends the Series/80 family of microcomputer products into a wide variety of instrumentation and process control applications.

The BLC-732 provides multiple analog input and output capability. The input function allows sampling of analog data at a rate of 50,000 samples per second and storage of equivalent digital values for subsequent processing. The BLC-732 is equipped with sample and hold circuitry, and accuracy of conversion is assured by holding the input sample constant until conversion is completed. The output function permits digital data conversion of 0 to ±10 volts analog in unipolar or bipolar output form.

Analog inputs may be sampled in random, sequential or single channel repetitive mode. The board contains high resolution 12-bit analog converters for input and output, 16 single-ended or 8 differential input channels, 2 output channels, programmable gain input amplifier and the sample and hold function. The analog input capacity is expandable to 32 single-ended or 16 differential channels.

The BLC-732 is a plug-compatible replacement for Intel's SBC-732.

Functional Description

Standard Series/80 instructions control analog input and output. Memory mapped I/O simplifies the programming task by permitting the transfer of data with simple memory reference instructions to predefined memory locations.

With memory mapped I/O, a segment of 16 contiguous addresses is predefined and set on the board. These addresses may be on any even 16 byte boundary within the 64K bytes of available address space. If these addresses overlay system memory addresses, memory inhibit logic prevents address contention for memory mapped I/O addresses.

Analog Input

Analog to digital (A/D) conversion is initiated by a Write command to the Multiplexer Address Register (MAR). The bit pattern of the MAR specifies the gain and the specific channel to be converted. The Command Register (CR) is then loaded with a bit pattern that enables conversion and the desired interrupts. Bits in the Command Register also specify pacer clock/external trigger, clearing, the board busy bit, and enabling sequential scan.

If the sequential scan feature is enabled, input channels will be sequentially converted until the channel address in the Last Channel Register (LCR) is reached.

Data sent to the Command Register can be read back by issuing a Read command to the Status Register (SR). In addition to verifying the last command word sent to the Command Register, the status also signifies that the last channel has been reached.

After analog conversion is complete, the corresponding digital data value is read from the converter register. The first byte contains the low order 4 bits (bits 0 to 3) of the digital representation; the second byte contains the 8 high order bits (bits 4 to 11).

The selected analog input is applied to the A/D converter through a software controlled programmable gain amplifier which provides gains of X1, X2, X4, or X8, and a sample and hold amplifier. With the A/D converter jumper selected for +5V, +10V, ±5V, or ±10V full scale input voltages, the gain amplifier permits sampling of analog input voltages as shown in Table I.

Table I. Programmable Gain Full Scale Values

Gain Selected	Voltage Range Selection			
	+5V	+10V	±5V	±10V
X1	+5V	+10V	±5V	±10V
X2	+2.5V	+5V	±2.5V	±5V
X4	+1.25V	+2.5V	±1.25V	±2.5V
X8	+0.625V	+1.25V	±0.625V	±1.25V

Sampling is controlled in one of three ways: by program instruction (writing the multiplexer address to an analog input channel), by an internal sample timer (pacer clock), or by external event synchronization (external trigger). The pacer clock may be jumper configured to provide timing intervals from 975 microseconds to 1 second.

Interrupts to the system CPU may be generated upon completion of either a channel sample conversion or a sequential channel scan. This relieves the system CPU of continuous status scanning.

The analog input control parameters are illustrated in Figure 1.

7	6	5	4	3	2	1	0
Gain Select	Gain Select	Not Used	2^4	2^3	2^2	2^1	2^0

Channel Select

Gain	Bit 7	Bit 6
X1	0	0
X2	0	1
X4	1	0
X8	1	1

a. Multiplexer Address and Gain Format

7	6	5	4	3	2	1	0
Not Used	Not Used	Not Used	2^4	2^3	2^2	2^1	2^0

Last Channel Address

b. Last Channel Sampled Address Format

7	6	5	4	3	2	1	0
Not Used	Not Used	End of Conv. Intrpt	End of Scan Intrpt	Clear Busy	Exit Trig Enable	Auto Incr Enable	Start/ Stop

c. Command Register Byte Format

7	6	5	4	3	2	1	0
Conv. Done	Scan Done	End of Conv. Intrpt	End of Scan Intrpt	Busy	Exit Trig Enabl	Auto Incr Enabl	Start/ Stop

d. Status Register Byte Format

7	6	5	4	3	2	1	0
Not Used	Not Used	Clear End of Conv. Intrpt	Clear End of Scan Intrpt	Clear Pacer Clock	Not Used	Not Used	Not Used

e. Clear Interrupts Format

Address	Write Command Description
Base + 0	Load Command Register (CR)
Base + 1	Load Multiplexer Address Register (MAR)
Base + 2	Load Last Channel Register (LCR)
Base + 3	Clear Interrupts

Address	Read Command Description
Base + 0	Read Status Register (SR)
Base + 1	Read Multiplexer Address Register (MAR)
Base + 4	Read LS Byte, A/D (ADCR)
Base + 5	Read MS Byte, A/D (ADCR)

f. Memory Mapped Addressing

Figure 1. Analog Control Parameters

Analog Output

The two independent analog outputs may be unipolar or bipolar and provide outputs from 0 to +5V, +10V, ±5V and ±10V using on-board jumper select options. Current mode output from 4 to 20 milliamps may be implemented by adding discrete resistors with the mode jumper set for unipolar operation. The current mode requires an external loop voltage of +15 to +30 volts. +15 volts may be derived from the on-board DC to DC converter.

The analog output is available when the most significant byte (the second byte) of the Write Command is transferred to the digital to analog channel hold register. Figure 2 illustrates the output parameters.

7	6	5	4	3	2	1	0
Data 11 (MSB)	Data 10	Data 9	Data 8	Data 7	Data 6	Data 5	Data 4

Second Byte (MS Byte)

7	6	5	4	3	2	1	0
Data 3	Data 2	Data 1	Data 0 (LSB)	0	0	0	0

First Byte (LS Byte)

Address	Write Command Description	Output Channel
Base + 8	Load LS Byte	0
Base + 9	Load MS Byte	0
Base + A	Load LS Byte	1
Base + B	Load MS Byte	1

Figure 2. Analog Output Control Parameters

DC to DC Converter

The board contains a DC to DC converter to convert the +5VDC power input to the ±15VDC required by analog circuitry. The converter input may be changed to permit the direct connection of external regulated voltages. This option is implemented with on-board jumpers and connection of the voltage via the auxiliary backplane connector.

Diagnostic Test

A diagnostic test program is included with the BLC-732 to allow testing and calibration of the analog circuits. Calibration is recommended when a channel full scale range jumper is set.

Specifications

Analog Input

Scan Mode — Sequential; Random; Single Channel Repeat

Channels — 16 single-ended or 8 differential

Channel Resolution — 12 bits

Full Scale Range Volts — 0 to +0.625; +1.25; +2.5; +5
0 to +1.25; +2.5; +5; +10
±0.625; ±1.25; ±2.5; ±5
±1.25; ±2.5; ±5; ±10

Programmable Gain — X1, X2, X4, X8

Sample and Hold —
- Aperture Time — Less than 100 nanoseconds
- Uncertainty Time — 20 nanoseconds
- Acquisition — 8 microseconds

Throughput Rate — 24 KHz

A/D Conversion Speed — 50 KHz

Overall Accuracy — (25°C)
Less than 0.05% FSR ± ½ LSB (Gain 1X)
Less than 0.07% FSR ± ½ LSB (Gain 2X, 4X, 8X)
[Includes 3 sigma noise, linearity, offset gain and dynamic response errors]

Input Impedance — 680 ohms (power off)
Greater than 100 megaohms (power on)

Input Current — 0 to 20ma (with 250 ohm user installed resistors)

Common Mode —
- Voltage — ±10.24V maximum (signal and common mode)
- Rejection — −60db (differential input) at source impedance
  Balanced — less than 5000 ohms
  Unbalanced — less than 1000 ohms

Crosstalk — −86db at 10 KHz

Overvoltage Protect — ±28VDC, AC peak

Temperature Coefficient — Less than 0.003% FSR/°C

Monotonicity — Guaranteed over the operating temperature range

External Trigger —	±4V for 200ns (min) with ⩽50ns rise time
Pacer Clock —	Crystal controlled, 0.05% accuracy Divider range $\frac{1000}{2^n}$ ms (n = 0 through 10)

Analog Outputs

Channels —	2 non-isolated
Channel Resolution —	12 bits including sign
Slew Rate —	10 volts per microsecond (no external capacitance)
Settling Time —	4 microseconds to ½ LSB
Accuracy —	0.05% FSR at 25°C (includes linearity and noise)
Temperature Coefficient —	0.005% FSR/°C
Monotonicity —	Guaranteed over operating temperature range

Other

Voltage Mode Output Characteristics —

Full Scale Range (Jumper select)	0 to +5V 0 to +10V 0 to ±5V 0 to ±10V 4 to 20ma
Output Current	±5ma at ±10V
Output Impedance	0.05 ohms
Output Capacitance	1000pf maximum

Current Mode Output Characteristics —

Full Scale Range	4 to 20ma current loop, unipolar (requires external loop voltage of 15 to 30 VDC)
Load Impedance	500 ohms maximum

System Bus Interface —	Data, address and command signals are TRI-STATE™ TTL compatible

Connectors —

System Bus	86 contact double-sided card cage edge connector on 0.156 inch centers
Analog	One 50 contact input double-sided edge connector on 0.1 inch centers Recommended mating connectors: 3M 3415-000, TIH312125 One 60 contact auxiliary double-sided edge connector on 0.1 inch centers Recommended mating connectors: CDC VPB01B30A00A2 AMP PES-14559 TIH 311130 One 50 contact input expansion double-sided edge connector on 0.1 inch centers Recommended mating connectors: 3M 3415-000, TIH 312113 or equivalent One 50 contact output double-sided edge connector on 0.1 inch centers Recommended mating connectors: 3M 3415-000, TIH 312125 or equivalent
Power —	+5V, 2.5A If Auxiliary Power is used: ±15VDC ±5%, 150ma
Environmental —	Temperature 0° to 55°C Humidity 0 to 90% non-condensing

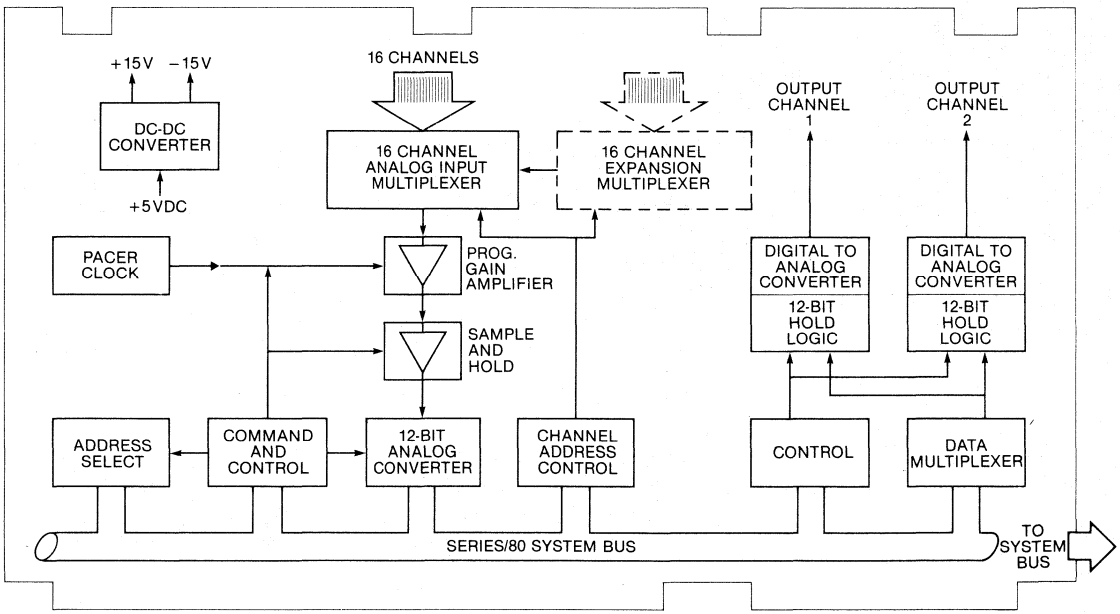
Physical —			
	Height	6.75 in.	(17.15 cm)
	Width	12.00 in.	(30.48 cm)
	Depth	0.50 in.	(1.27 cm)
	Weight	18 oz.	(510.3 g)

Order Information

BLC-732	Combination Analog I/O Board Includes 16 single-ended or 8 differential analog input channels and 2 analog output channels, manual and diagnostic test program in paper tape media

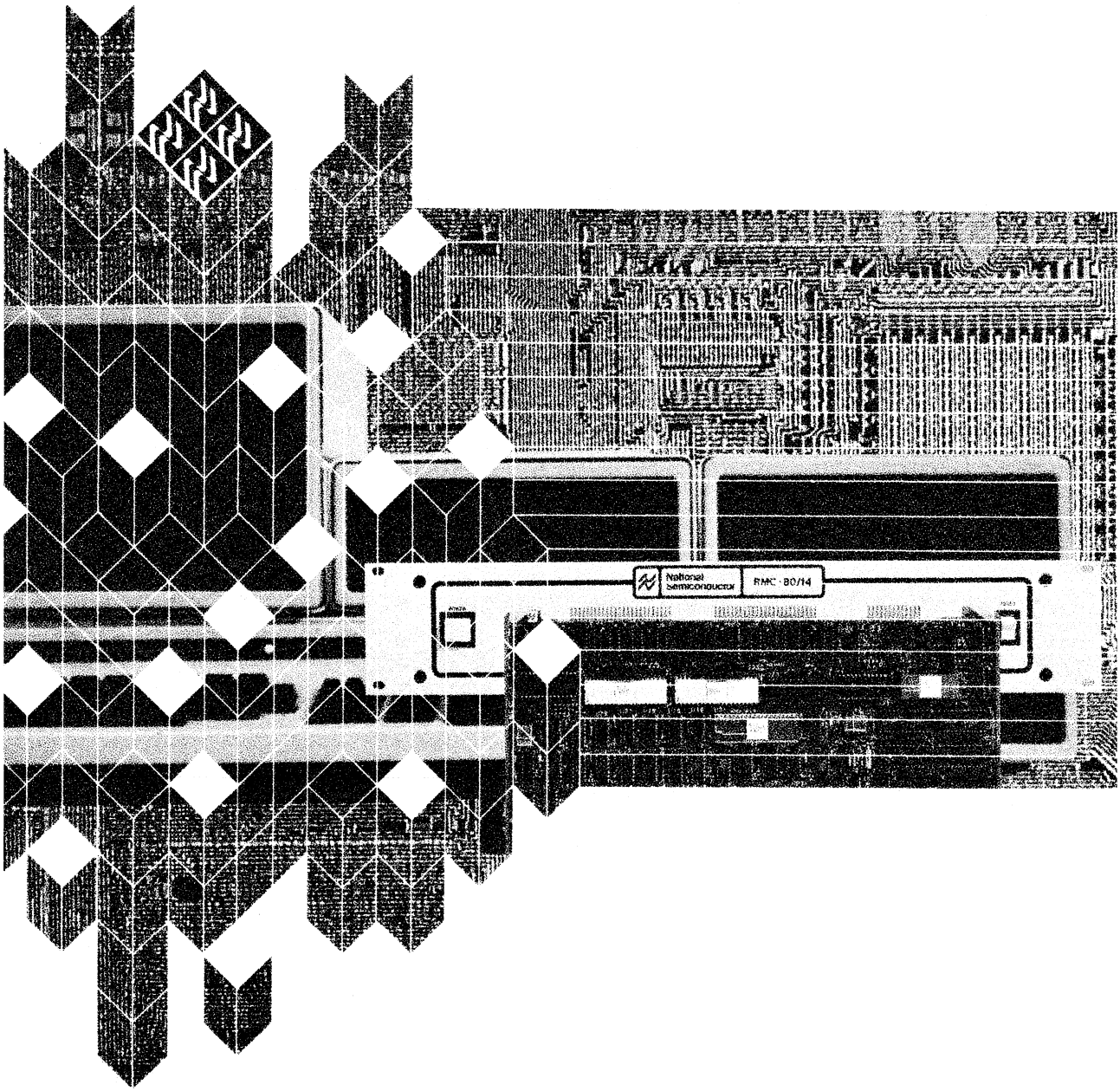
Documentation

420305649-001	BLC-711 and BLC-732 Analog Input and Combination Input/Output Board Hardware Reference Manual

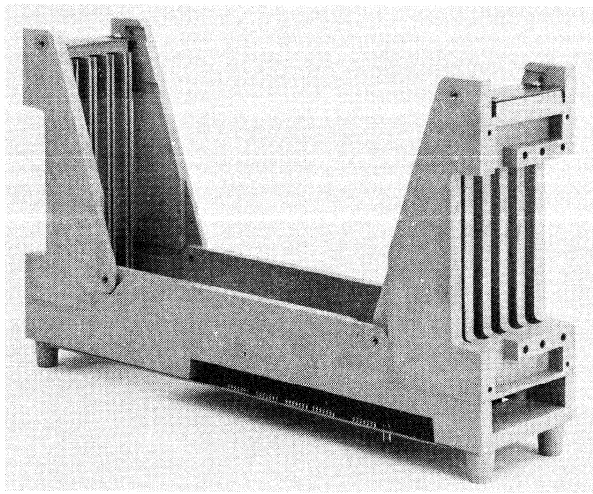


BLC-732 Diagram

Section 8
Chassis and Power Supplies



BLC-604 and BLC-614 Card Cages



- **Series/80 System Flexibility**
  - 4 board incremental expansion capability
  - Requires only 3.5 inches of vertical space
- **Easy to Use — Includes:**
  - Backplane
  - Power supply connector
  - Threaded mounting holes

Product Overview

The BLC-604 and BLC-614 System Card Cages are ready-made, low-cost chassis for the housing and interconnection of National Semiconductor's Series/80 Board Level Computer products. Both the BLC-604 and BLC-614 Card Cages hold up to four Series/80 boards. The BLC-604 may be used in a stand alone configuration, while the BLC-614 is used as an addition to the BLC-604 when more space is required.

Functional Description

The BLC-604 is a 4-slot molded chassis including a backplane, with data, address and control signal bus, terminating networks, power supply connectors, and a bus extension circuit card edge connector. When more than one card cage is necessary a four slot BLC-614 expansion card cage is plugged into the bus expansion connector on the BLC-604. The BLC-614 contains an expansion connector for cascading additional BLC-614 card cages. The number of card cages to be cascaded is limited only by the bus drive capability or space limitations of the system. A BLC-604 or BLC-614 occupies only 3.5 vertical inches permitting highly compact packaging. The card cages can be conveniently mounted in any one of three planes.

Optionally available to support Series/80 systems are the 14 Amp BLC-635 Power Supply or 30 Amp BLC-665 Power Supply. Both power supplies include cables for connection to the BLC-604 and BLC-614. Also available is a power supply cable kit, the BLC-957, containing 2-foot cables for custom power supply connection to the card cage.

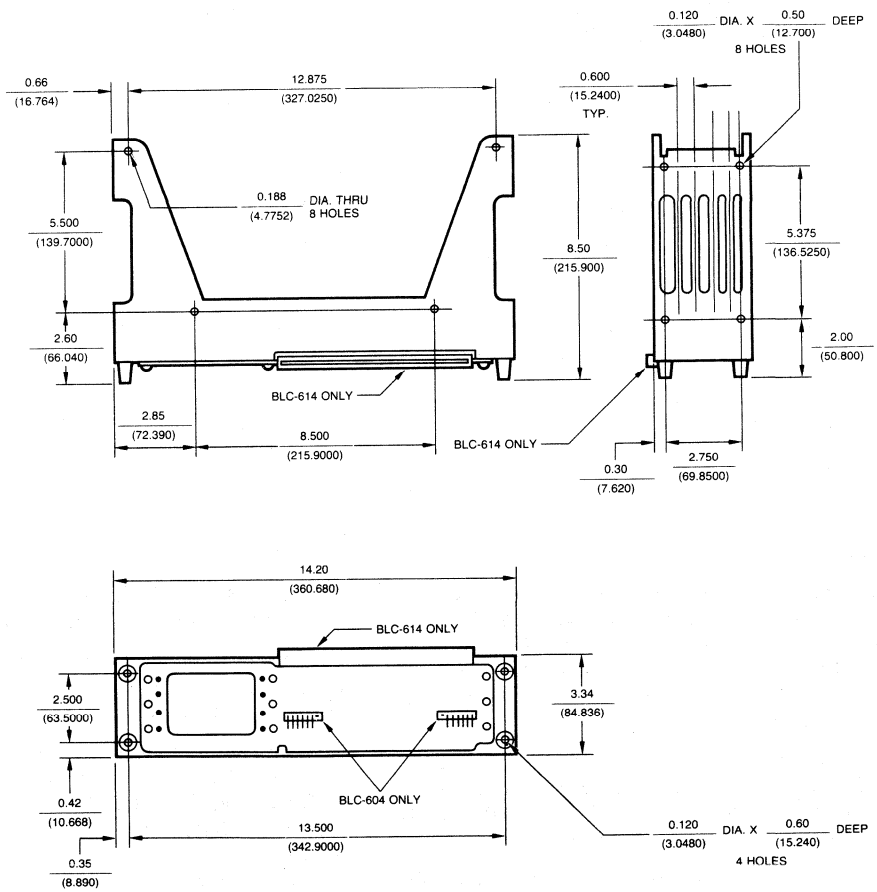
Specifications

Bus Connectors

Signal	86 contact double-sided card cage edge connectors on 0.156 inch centers		
Power	7-pin wafer with key (Molex crimp type 09-50-7071 or equivalent)		
Environmental —	Temperature 0° to 55°C		
	Humidity 0 to 90% non-condensing		
Physical —	Height	8.5 in.	(21.59 cm)
	Width	14.2 in.	(36.07 cm)
	Depth	3.34 in.	(8.48 cm)
	Weight	2.2 lbs.	(997.92 g)

Order Information

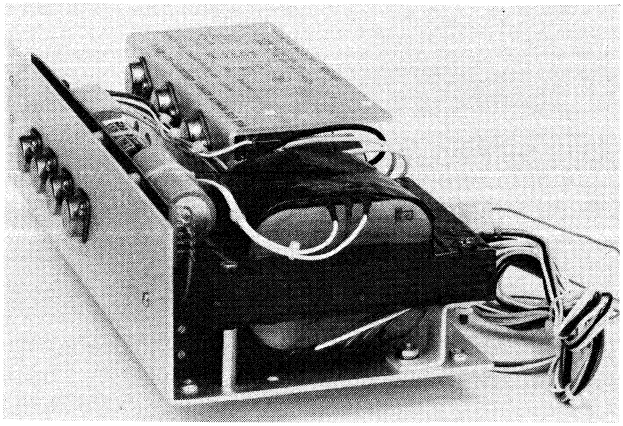
BLC-604	Card Cage and Backplane Assembly
BLC-614	Expansion Card Cage Assembly
BLC-957	Power Supply Cable Kit

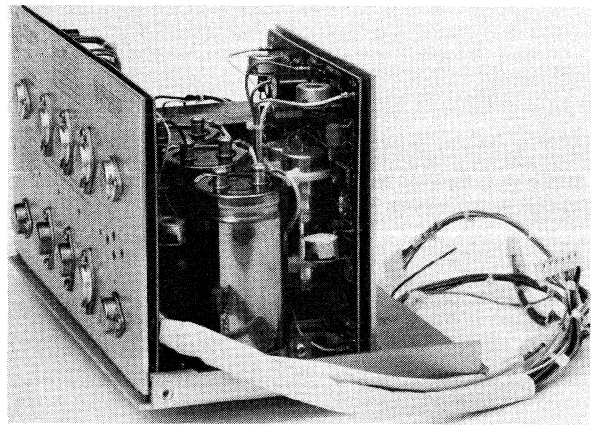


BLC-604 and BLC-614 Diagram

National Semiconductor

BLC-635 and BLC-665 Series/80 Power Supplies





- **Complete Power Supply Systems**
  - ±5, ±12 volt outputs
  - 110-115, 220-230 VAC input power
  - 47-63 Hz input frequency
- **High System Reliability**
  - AC low voltage sensing with TTL level output signal
  - Current limited outputs
  - Output overvoltage protection
- **Compatible with BLC/SBC Series/80 Systems**
  - BLC-635 supplies BLC/SBC CPU and three expansion boards
  - BLC-665 supplies BLC/SBC CPU and seven expansion boards
  - Mating cables for BLC/SBC-604 and 614 System Card Cages
  - BLC-635 — plug-replacement for SBC-635

Product Overview

The BLC-635 and BLC-665 are ready-made, low-cost power supplies for National Semiconductor's Series/80 Board Level Computers. These power supplies provide ±5 and ±12 volts of regulated DC power at maximum current over a temperature range of 0° to +55°C.

The BLC-635 provides power for a fully loaded BLC/SBC CPU with enough additional capacity to supply most configurations of three BLC/SBC memory, I/O, or other expansion boards.

The BLC-665 supplies approximately twice the rated power of the BLC-635. The BLC-665 will power a fully loaded BLC/SBC CPU board and most combinations of seven additional expansion boards.

All outputs are current limited and have overvoltage protection. The AC input is fused for either 100-115 VAC or 200-230 VAC operation.

DC power is carried on cables keyed for compatibility to the BLC-604 System Card Cage. The BLC-635 and BLC-665 utilize circuitry to sense an AC power failure or low line conditions and will generate a TTL compatible signal for orderly system shutdown.

Functional Description

Output Current Rating

VDC	BLC-635	BLC-665
+5	14 A	30 A
−5	0.9 A	1.75 A
+12	2.0 A	4.5 A
−12	0.8 A	1.75 A

Current limit approximately 20% above rated values.

Output Adjust Range

±5% minimum on all outputs around nominal voltage

Line Regulation

±0.1% on all outputs for 10% line change

Load Regulation

±0.1% on all outputs for 50% load change

Output Ripple and Noise

10 mv peak-to-peak maximum on all outputs from DC to 500 KHz

Stability

±0.05% on all outputs for 8 hours at constant line, load, and temperature after 30 minutes of warm-up

Transient Response

±5% on all outputs maximum for less than 50 microseconds with 50% load change

Remote Sensing

Provided at P8 connector for +5 volts

Chassis Ground Insulation

All output returns isolated from chassis ground

Overvoltage Protection

Provided on all outputs and factory set to trip within the following ranges:

Output Voltage	OVP Trip Range
+5V	5.8V to 6.6V
−5V	−5.8V to −6.6V
+12V	14V to 16V
−12V	−14V to −16V

Overload and Short Circuit Protection

+5V — Foldback current limiting with automatic recovery

−5V, +12V, −12V — Current limited to extent no damage will occur for extended overload condition

---

Specifications

Input Power — 100, 115, 215, 230 VAC ± 10%
47-63 Hz

Input Fusing — 100/115 VAC 3.0 A slow blow
200/230 VAC 1.5 A slow blow

Connectors —

	BLC-635/665 Connectors			Recommended Mating Parts		
		Part Number			Part Number	
	Type	Molex	Amp	Type	Molex	Amp
AC Input (P2)	Connector Pin	03-09-2052 02-09-2118	N/A	Connector Pin	08-09-1052 02-09-1118	N/A
DC Output (P6, P8)	Connector Pin Polarizing Key	09-50-7071 08-50-0106 15-04-0219	87159-7 87023-1 87116-2	Right Angle Connector Assembly	09-66-1071	87194-6
"AC Low" Detection (J3)	Connector Assembly	09-67-1072 or 09-66-1071	87262-7	Connector Pin Polarizing Key	09-50-7071 08-50-0106 15-04-0219	87159-7 87023-1 87116-2

Environmental — Temperature 0° to 55°C
Humidity 0 to 90%
non-condensing

Physical —

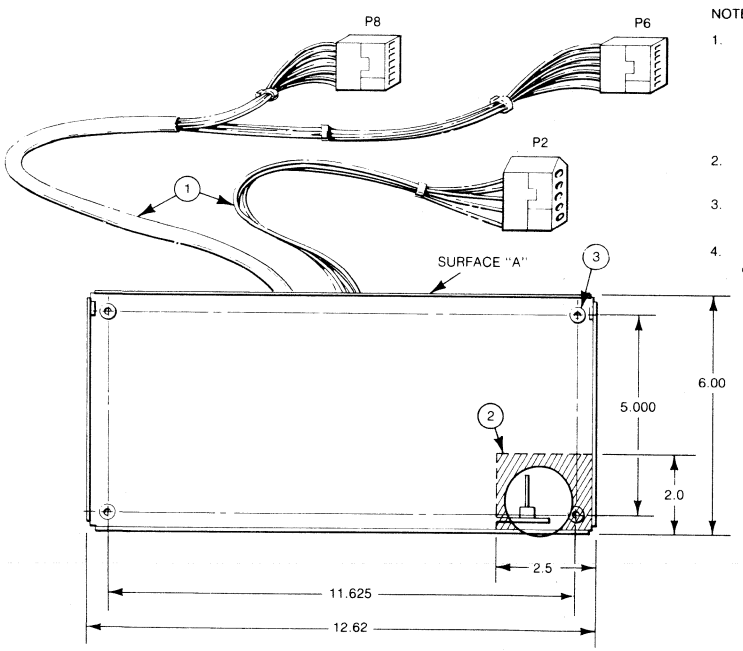
	BLC-635	BLC-665
Height	3.19 in. (8.1 cm)	6.62 in. (16.8 cm)
Width	6.03 in. (15.3 cm)	6.50 in. (16.5 cm)
Depth	12.65 in. (32.1 cm)	12.65 in. (32.1 cm)
Weight	13 lb. (5.9 kg)	21 lb. (9.6 kg)

Order Information

BLC-635	14 A Power Supply, includes cables for connection to card cage.
BLC-665	30 A Power Supply, includes cables for connection to card cage.

Documentation

420305489-001	BLC-635 Power Supply User's Manual
420305220-001	BLC-665 Power Supply User's Manual

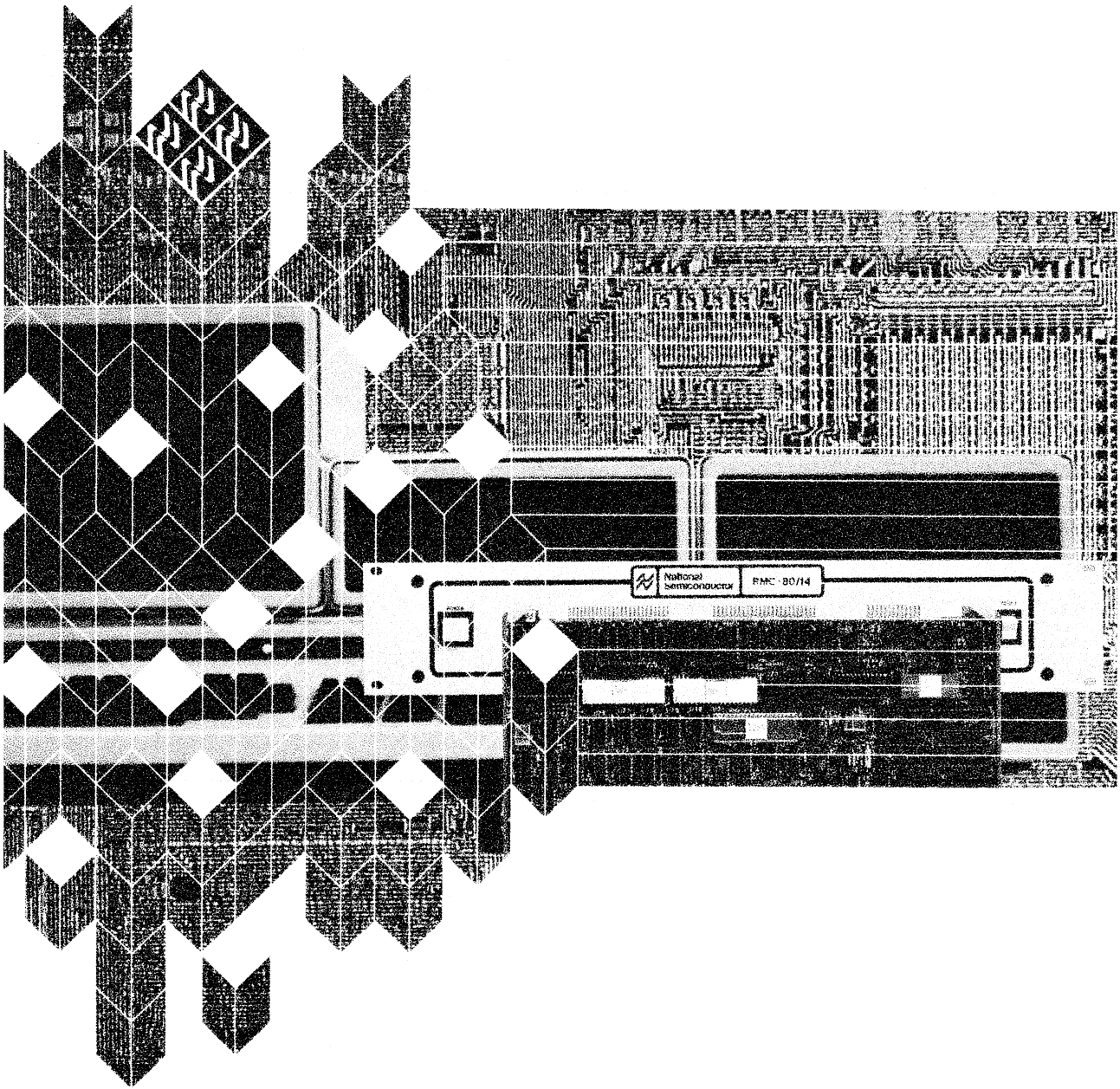


NOTES:

1. Harness lengths are from center of surface "A" to connector
   a. DC OUTPUT 24 inches to P6 conn.
   b. DC OUTPUT 16 inches to P8 conn.
   c. AC INPUT 12 inches to P2 conn.
2. Location of "AC LOW" signal connector is within cross hatched volume, orientation may vary.
3. All four mounting holes threaded for 8-32 machine screws.
4. BLC-665 has 2 each connectors P6, P8 to enable connection to two card cages.

BLC-635 and BLC-665 Diagram

Section 9
Development System



STARPLEX™ Development System

- **A Total Development System**
  - Hardware:
    CPU, Floppy Discs, Video Monitor, Keyboard, Printer
  - Software:
    Disc Operating System, Debugger, Editor, Macro Assembler, FORTRAN, BASIC, On-Board ROM Diagnostic and Utilities
  - Options:
    In-system emulator, PROM programmer
- **Easy to Use**
  - Function keys direct system
  - Prompting menus guide operator entries
  - Comprehensible error messages
  - Keystroke-driven editor
- **Full National Semiconductor Product Line Support**
  - Supports 8080-based microprocessor systems and BLC/SBC microcomputers
  - Expandable with industry standard BLC/SBC boards

Product Overview

The STARPLEX™ Development System is a general purpose microcomputer and microprocessor development system. New levels of operating simplicity have been designed into the STARPLEX system to significantly reduce the amount of time spent on product development. By getting the user into actual application work sooner and with fewer mistakes, the STARPLEX system allows the user to take full advantage of time spent at the console.

A Total System

The STARPLEX design combines all the components required for the entire development task in one complete system. The STARPLEX package includes an 8080-based CPU board, 64K bytes of RAM, 512K bytes of disc storage, a video monitor, keyboard and printer. The standard STARPLEX software package includes a disc operating system, assembler, debugger, editor, linker, loader, FORTRAN, BASIC, on-board ROM diagnostic and utilities. Two options are available: an in-system emulator for real-time debugging of customized hardware and software and a PROM programmer personality module for programming, verifying and copying PROM's.

Easy to Use

The STARPLEX System reduces the time a user must spend at a terminal by making many complex functions accessible through one easy keystroke. System commands are initiated by clearly marked function keys which invoke prompting menus to guide the user through each task. These function keys eliminate the need to memorize system commands and various command options. As a result, there is no need to refer to lengthy documentation, and errors or delays caused by incorrectly entered commands are eliminated.

Recognizing that a great deal of the user's time is spent on creating and changing source code, the designers of the STARPLEX system have devoted special attention to the text editing facility.

A set of special function keys directs the STARPLEX editor, allowing corrections to be made with single keystrokes. An entire file may be quickly and easily reviewed or altered. The number of mistakes is reduced because the data and changes are immediately displayed. Backup files are automatically created, protecting the user from accidental loss of data. Because the STARPLEX system is easy to use, learning time is considerably shortened. A first time user can be productive within a half hour. Also, as users make more efficient use of the system, machine availability is maximized.

Full Product Line Support

When a user buys a STARPLEX System he can be assured it will meet both today's and tomorrow's development needs. All the boards within the STARPLEX System are members of National's Series/80 family and use the standard Series/80 bus, making the system expandable with the more than 40 boards presently available in this series.

The STARPLEX System presently supports development for the 8080A microprocessor and will support all future National microcomputer and microprocessor products as well.

The Result — Cost Effectiveness

The most important feature of the STARPLEX System is that it saves development time. Its ease of use allows the designer to concentrate on solving the application problem, rather than learning how to operate the system. With the STARPLEX system, the effectiveness of a company's most valuable resource — "engineering manpower" — is maximized.

Functional Description

Hardware Modules

STARPLEX components are packaged into modules which form a unified system when placed together. The modules are durable, with housings constructed of 1/8 inch aluminum and front panels of molded lexan foam.

STARPLEX is designed for easy maintanance. Snap-down doors on the base module make it easy to access the card cages and circuit boards. Interconnecting cables between all modules and boards are routed to the rear of the system and covered by easily removable cable channels. Thus, cables are out of sight and protected from accidental damage. All cables, including the single AC power distribution system, are plug detachable at both ends, making it easy to disconnect modules and reconfigure the system.

Human engineering concepts have directed the design of each STARPLEX module to make the man-machine interface as natural as possible. For example, the video monitor screen has antireflective coating to minimize glare, and light-emitting diodes in certain keys provide operator awareness of their selection. Even cooling fans have been located to minimize noise levels.

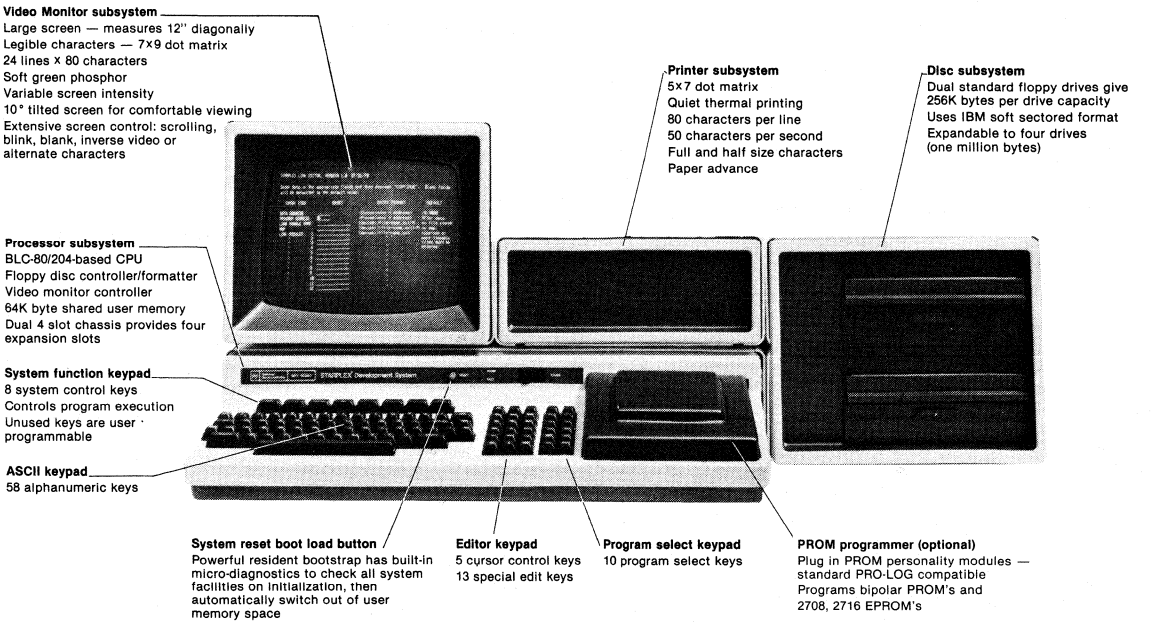
STARPLEX Electronics

Four Series/80 boards make up the STARPLEX electronics: the main CPU board (based on the BLC-80/204), the video monitor/keyboard controller (BLC-8229), the floppy disc controller (BLC-8221) and a 64K memory board (BLC-064).

These boards communicate with each other via the standard BLC system bus. The CPU, BLC-8229 and BLC-8221 all have multi-master bus logic on their respective boards allowing them to share the system bus. The BLC-8229 and BLC-8221 can communicate with the CPU using either Direct Memory Access or programmed I/O.

The thermal printer and optional PROM programmer personality module communicate with the CPU through two programmable parallel I/O ports. An RS232C port on the CPU is available and permits both asynchronous and synchronous communications for use with a printer or a communications device.

Individual circuit boards are built to National's high manufacturing quality standards, utilizing techniques such as computer aided layout and auto insertion. All boards and the system as a whole are tested dynamically under system load conditions at elevated temperatures as part of a thorough factory burn-in.



CPU

The host CPU board in the STARPLEX system is based on the BLC-80/204.

- 8080A CPU
- Multi-master bus control
- Up to six masters with serial priority
- Sockets for 4K or 8K x 8 PROM
- 48 programmable I/O lines
- Buffered address and data lines
- Programmable RS232C communications interface with software selectable baud rates
- Eight-level programmable vectored interrupts
- Three programmable timers

BLC-064

- 64K Random Access Memory
- On-board refresh timing and control
- Refresh synchronized with CPU

BLC-8229 — Video Monitor/Keyboard Controller

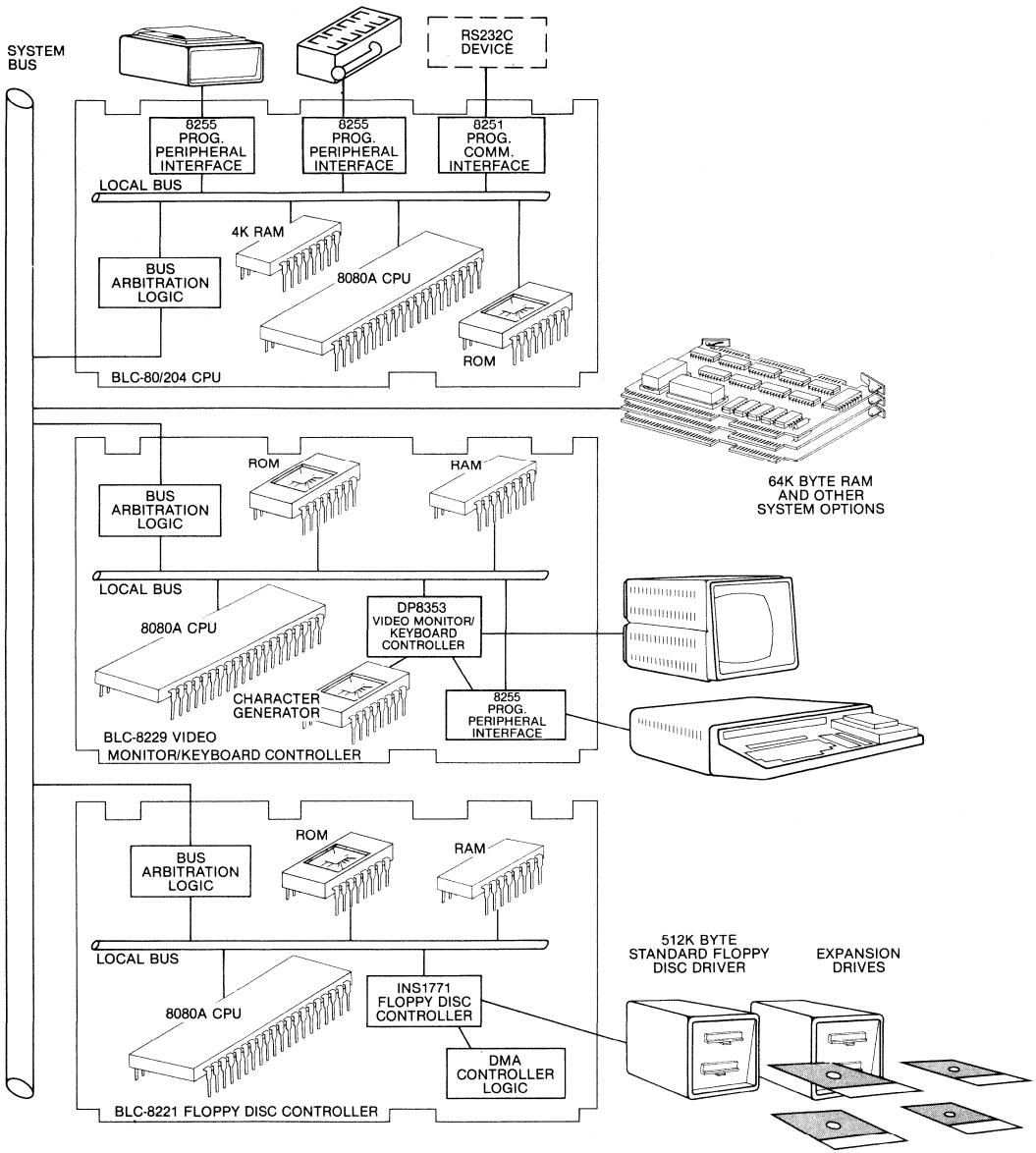
The BLC-8229 provides full video monitor and keyboard interface capabilities on a single board.

- Microprocessor controller (8080A)
- 4K ROM
- 1K RAM
- 24 lines by 80 characters
- Full multi-master capabilities
- Display attributes — blink, blank, inverse video, alternate character set
- 128 character set stored in local PROM

BLC-8221 — Floppy Disc Controller

The BLC-8221 provides the interface for the floppy disc module.

- Microprocessor controlled (8080A)
- Supports up to four drives
- Soft sectoring
- Formatting controlled by on-board firmware (4K PROM)
- CRC on-board
- 1K RAM data buffer
- Full multi-master capabilities



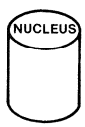
STARPLEX Multiprocessor System Diagram

Software

STARPLEX software is completely thought out from a functional standpoint, carefully engineered to be easy to understand and use and thoroughly integrated into the total system. Every aspect is designed to assist the user in rapidly developing microprocessor-based systems from the ground up.

The elegance of STARPLEX software lies in its ability to make the complicated process of program development appear simple to the user.

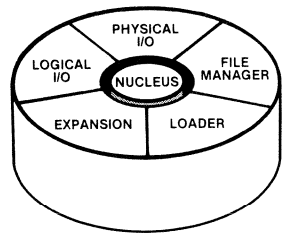
The software system is structured as a series of rings around a nucleus. Segments of these rings can be changed or added for future development requirements such as other high-level languages, file handlers or special user-defined routines.



NUCLEUS

The nucleus of the STARPLEX operating system controls and allocates system resources for the higher level processes.

- Provides synchronization and communication facilities for higher level asynchronous processes
- Services all hardware interrupts
- Provides interval timer functions
- Completely device-independent



LEVEL I

Level I of the operating system provides system housekeeping functions and coordinates access to system resources. It includes a file manager, an I/O control system and a loader.

File Manager

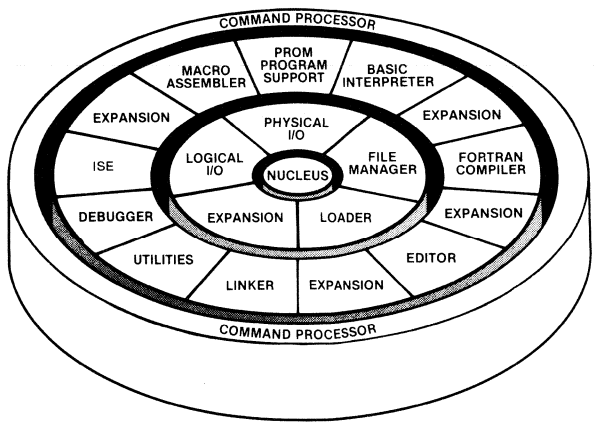
The file manager organizes, stores and retrieves data and programs stored on the diskette.

- Maintains a directory
- Allows multiple file attributes
- Uses a "hierarchical linked list" structure
- Supports random access

I/O Control System

The I/O control system is designed to eliminate the need for the user to understand the physical I/O characteristics of each individual device and presents a simplified, logical device-independent architecture.

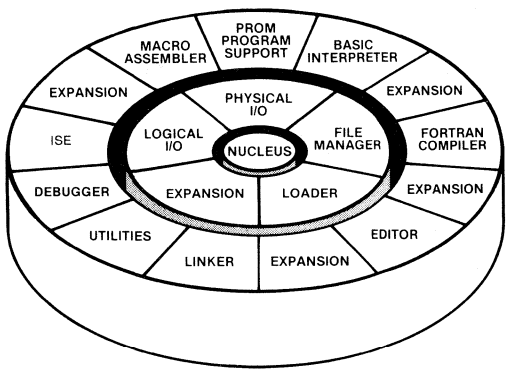
- Provides overlapped I/O commands
- Allows files to be accessed by name
- Handles error conditions



Loader

The loader brings programs into main memory at specified locations.

- Provides "load and go" mode
- Allows controlled load mode — starting address returned to calling program



LEVEL 2

Level 2 of the operating system provides the "development services" including a linker, a CRT-oriented editor, utilities, a debugger, PROM programmer support, a Macro assembler, BASIC and FORTRAN IV.

Linker

The linker combines selected relocatable object modules created by the assembler or language compiler into an executable run time module.

- Assigns absolute addresses to load modules
- Produces a memory map of linked components
- Searches system and user libraries for unresolved external references

Editor

The STARPLEX editor is an easy-to-use CRT-oriented text editor.

- Function key driven
- Forward and backward paging
- Automatic source file backup
- Traps illegal commands

Utilities

General utilities provide routine maintenance functions.

- Transfer data files between devices
- Obtain diskette directory listings
- Format diskettes
- Modify file attributes
- Rename files

Debugger

The program debugger simplifies program checkout by allowing program execution to be monitored and altered.

- Allows single step control
- Permits eight breakpoint assignments
- Displays program counter and registers at breakpoints
- Memory references are absolute or relative to one of the relocation registers

PROM Programmer Support

The PROM programmer support software manages the optional PROM personality module functions.

- Allows PROM code to be listed, verified and copied
- Data stored in a PROM can be transferred to or from another PROM, a diskette file, memory, the video monitor or keyboard.

Macro Assembler

The Macro assembler assembles 8080A mnemonic code and allows operator definition of useful higher level instructions called "Macros" which are then expanded into a sequence of machine level instructions.

- Generates absolute or relocatable object modules
- Conditional assembly parameters
- Allows external references

FORTRAN IV

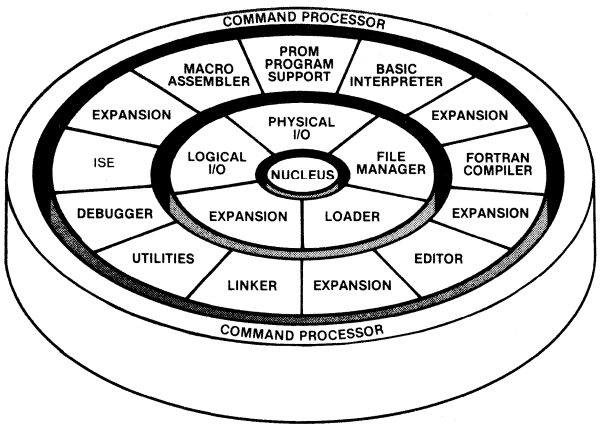
The FORTRAN IV compiler on the STARPLEX system meets the ANSI X3.9-1966 standard and includes the following enhancements:

- PEEK and POKE — allow direct access to memory
- INP and OUT — allow direct I/O access
- Comprehensive subroutine library
- Supports user-written I/O drivers
- Random access disc I/O
- Allows assembly language subroutine calls

BASIC

The STARPLEX BASIC compiler/interpreter conforms to the Dartmouth defined BASIC with extensions:

- PEEK and POKE — allow direct access to memory
- INP and OUT — allow direct I/O access
- Complete string operators
- Multi-dimensional arrays
- Extensive debugging and programming aids — trace, edit, direct mode, renumber



LEVEL 3

The Command Interpreter is the interface between the operating system and the human operator.

- Function key driven
- Verifies user requests
- Provides menus and prompting for system commands

Specifications

Memory —	64K bytes
Floppy Disc —	
Format	IBM compatible, soft-sectored
Capacity	256K bytes per drive
Maximum Capacity	1 million bytes (4 drives)
Printer —	
Type	Thermal
Speed	50 characters per second
Width	80 columns
Character Type	5x7 dot matrix
Video Monitor —	
Matrix	7x9 dot
Display Array	80 columns by 25 lines
Phosphor	P2 green
Power —	115VAC, 60Hz, 10 amps (max) or 230VAC, 50Hz, 5 amps (max)
Base Module	644 Watts
Floppy Disc Module	966 Watts
Thermal Printer	126 Watts
Video Monitor	34 Watts

Physical —

	Base Module	Floppy Disc Module	Thermal Printer	Video Monitor
Height	5.75 in. 14.6 cm	11.5 in. 29.2 cm	5.75 in. 14.6 cm	11.5 in. 29.2 cm
Width	26 in. 66 cm	13 in. 33 cm	13 in. 33 cm	13 in. 33 cm
Depth	26 in. 66 cm	19 in. 48.3 cm	19 in. 48.3 cm	19 in. 48.3 cm
Weight	68 lb. 30.8 kg	50 lb. 22.7 kg	28 lb. 12.7 kg	29 lb. 13.2 kg

Order Information

SPX-80/40	STARPLEX Development System (60 Hz)
SPX-80/40E	STARPLEX Development System (50 Hz)

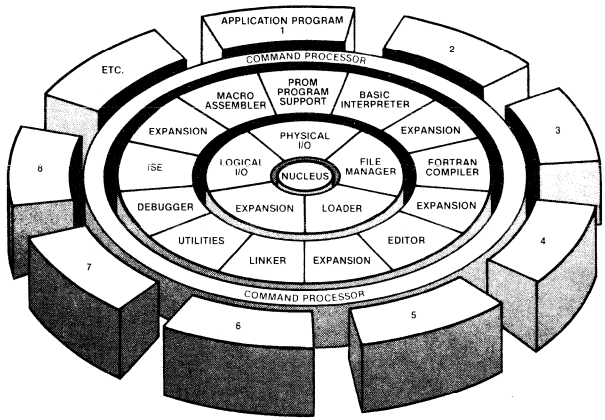
Options

SPM-A02-1	PROM programming module for programming 2708 EPROM's in a STARPLEX Development System
SPM-A02-2	PROM programming module for programming 2716 EPROM's in a STARPLEX Development System
SPM-A02-3	PROM programming module for programming National 74S and 87S type bipolar EPROM's in a STARPLEX Development System

Documentation Included with SPX-80/40 and SPX-80/40E

420305546-001	STARPLEX System Reference Manual
420305788-001	STARPLEX System Software Reference Manual
420305789-001	STARPLEX Macro Assembler Software User's Manual
420305790-001	STARPLEX FORTRAN Compiler Software User's Manual
420305791-001	STARPLEX BASIC Interpreter Software User's Manual
420305586-001	BLC-8201/8221 Floppy Disc Controller Hardware Reference Manual
420305587-001	BLC-8228/8229 Video Monitor/ Keyboard Controller Hardware Reference Manual
420305916-001	STARPLEX Quick Reference Guide
420305793-001	STARPLEX Hardware Maintenance Manual
420305521-001	BLC-80/204 Board Level Computer Hardware Reference Manual
420305529-001	BLC-032/048/064 32/48/64K RAM Board Hardware Reference Manual

STARPLEX™ Disc Operating System



- **Complete Self-Contained System**
  - Full support of all hardware
  - Complete array of software tools
- **Simplified Program and User Access to All Peripherals**
  - Device-independent I/O
  - Dynamic logical unit assignment
  - Names files and devices
- **Convenient Control Facilities**
  - Special function keypads
  - Single keystroke command functions
- **User-Oriented Support Programs**
  - Editor controlled by special function keys
  - High level languages for rapid application program development
  - English language error messages
- **Full Set of Utilities**
  - Linker — allows modular program construction
  - Loader — locates programs on disc and loads them into memory
  - Debugger — minimizes program checkout time

Product Overview

Yesterday's development systems were designed with only one aspect of the development function in mind — the hardware. Today people, not hardware, are the most costly element of the development process, and development systems now must maximize the utility of the human resource.

The STARPLEX Disc Operating System (DOS) is a general purpose, user-oriented software system designed to eliminate tedious time-consuming tasks normally associated with program preparation, debugging and maintenance. All software required to develop, debug and maintain user applications in Assembler Language, FORTRAN IV, and BASIC is provided with the STARPLEX System. The software includes: an Editor for creating/editing source files; high level languages for easy program implementation; a Macro Assembler for generating absolute/relocatable object modules; an I/O management system for accessing and controlling peripheral devices; a Linker for gathering all program modules into a run file; a PROM programmer support package and a program debugger for run time program testing.

One of the key design features of the STARPLEX DOS is its ease of use. The special function keypads make access to the operating system,

languages and system utilities as easy as a single keystroke. With STARPLEX DOS it is not necessary to wade through lengthy instruction manuals in order to perform a simple operation; instead, the clearly labeled function keys perform complex and repetitive functions without requiring the operator to memorize awkward command structures.

Specially designed screen menus augment the special function keys. Press a key and a menu of commands appears on the CRT screen. This menu has fill-in-the-blank fields that define the information needed from the operator in order to perform the function. By using the TAB key the user selects the function and fills in the necessary information. Pressing the RETURN key signals the system to take action. The standard system menus may be modified to suit individual needs or entirely new menus created to fit the application problem.

The extensive and easy-to-use system and program control features, utility functions and data management facilities free the user to concentrate on problem-solving rather than system management.

Functional Description

The STARPLEX Disc Operating System is structured as a series of layers, each inner layer providing program services to the outer layers.

The nucleus forms the central core of the system. Its primary function is to provide synchronization and communication facilities for higher level processes. This is accomplished by a set of queues and associated operations used to implement a message passing structure for communication to and from the outer layers. In this manner the nucleus controls and allocates system resources for the higher level processes.

The first layer around the nucleus provides system housekeeping functions and consists of a file manager, input/output control system and a program loader. This layer coordinates access to system resources and relieves higher level functions of the need to specify the particular characteristics of the various input and output resources.

The next layer provides utilities and interface to higher level languages. Finally, the command processor at the outer edge is the interface between the operating system and the human operator. It responds to keyboard commands, checks their validity and invokes the appropriate system service requests.

System Function Keys

In order to simplify user control and access, several special function keypads have been provided. These keypads allow the user to call complex or time-critical functions with a single keystroke. Keys are provided to PAUSE and CONTINUE system activity, END or ABORT programs, invoke the EDITOR, FORTRAN compiler, Macro Assembler, Linker, BASIC interpreter and other utility programs, and request help from the system. When appropriate, the command processor will ask for supplementary information such as file name or for confirmation of the command.

I/O Control System

The input/output control system is designed to relieve the user of the need to understand the physical I/O characteristics of each individual device, and is implemented at two levels. At one level the program interface is to a logical input/output device, allowing a program to be device-independent. This method permits the user to redirect output of a program to any available device at run time without having to re-compile or re-assemble the program. This often results in significant time savings in the program debug phase. The second level is the physical device driver interface. At this level the logical I/O service routine communicates with the device driver and translates the logical I/O request to device characteristics. Direct calls to the device driver also allow the user full access to individual device characteristics for special applications problems.

The I/O processor provides several I/O calls at the system level to maximize the flexibility of the system. READ and WRITE calls transfer data between the specified device and main system memory. Control is returned to the calling program after completion of the I/O transfer. To provide greater system design flexibility two additional I/O calls (READ INITIATE and WRITE INITIATE) are provided that allow overlapped I/O. READI and WRITI calls initiate I/O processing but return control to the calling program without waiting for the I/O process to be completed. The calling program can later check for an I/O-complete status using an IOCHK call or place itself in a "wait for completion" state with IOWAIT.

Set keyboard mask (KBDMSK) is another facility that adds significant flexibility to system design. This service allows the calling program to specify which keys the system should accept and which keys should be responded to with an error tone. KBDMSK allows the program to dynamically change the keyboard environment according to the

current program mode needed. The STARPLEX editor uses this facility extensively to control inputs to the various editing modes. This capability may also be used to specify that the program itself wishes to control and respond to system functions such as ABORT, END, CONTINUE, PAUSE and HELP.

File Management

File Structure:

Files in STARPLEX are identified by a three part file descriptor consisting of volume name, file name, and extension. An example of a file descriptor is FDS:PROG.FOR, which specifies a disc known to the system as "FDS" and a FORTRAN source file named PROG.

The indexed file structure allows the manipulation of logical records that are automatically blocked and deblocked. These logical records can be accessed one after the other by sequential I/O calls or randomly by specifying a logical record number. The indexed file is open-ended, does not require pre-allocation of disc space, and allows new data to be appended to it. Files may be allocated, named, deleted, renamed or protected by operator command or program control. This capability enables programs to dynamically change the operating environment and results in greater flexibility.

File Protection:

Three types of protection attributes are available. Files may be designated as write protected so that no program may write over the stored data. A transparent mode designates permanent or semi-permanent files that are not listed when the DIRECTORY LIST command is executed, unless specifically requested. This significantly shortens the list the operator normally reviews in the program development process. The third protection attribute specifies a permanent mode. Files designated as permanent may not be deleted.

Editor

The STARPLEX System Editor is a powerful system tool for the creation and maintenance of source code. The Editor may be used to generate and modify source text for any programming language as well as data files and screen formats.

A special Editor keypad is provided that reduces most Editor command functions to a single keystroke instead of long and complicated command syntax. Using this keypad the operator can insert or delete characters or lines, scroll through the text file forward or backward a line or a page at a time, position the cursor and set tabs simply by pressing a key. By reducing the keyboard operations almost exclusively to data input, the STARPLEX Editor makes maximum use of the operator's time.

Linker

The Linker combines selected relocatable object modules created by the assembler or language compiler into an executable run time module. System libraries and user-specified libraries are searched to satisfy any unresolved external references. A comprehensive load map may be generated which lists resolved and unresolved external references with their memory locations.

It is possible to specify that sections of a program be loaded into absolute or relative segments of memory. This allows separation of data and program code when linking programs for RAM destinations or when creating a module for the programming of PROM's.

Loader

The loader brings programs and data into main memory at specified memory locations. If the object file is relocatable it loads the file and performs the translation from relocatable to absolute format. After loading, the loader provides for direct execution (load and go) or controlled execution (load only) by the calling program.

Macro Assembler

The Macro Assembler generates absolute or relocatable object modules from instruction statements and directives. Listings may be generated which include original source statements, machine code with memory address (absolute or relocatable), and a list of referenced symbols. External statements are provided to permit separately generated modules to reference one another and have addresses resolved at link time. Conditional assembly directives direct the assembler to assemble or ignore certain sections of code. Macros simplify generation of repetitive code and standard subroutines and provide the vehicle for standardizing system calls.

Debugger

Program execution may be monitored and altered through the use of the system debugger. Memory references are absolute or relative to one of the eight relocation registers. The program counter, accumulator, memory and all hardware register contents may be inspected and changed. Programs may be executed at full speed or flow traced by using the single step function. Multiple breakpoint capability is provided with automatic content save

and restore. When used, breakpoints transfer control to the debugger as they are encountered during program execution and are automatically restored after breakpoint execution.

General Utilities

Utility programs provide file maintenance capabilities such as copy, rename, delete and reprotect. The transfer of information between devices is handled by the "copy" function. For example, to display a file simply "copy" the file to the video monitor. A complete roster of files may be obtained which lists the names, protection attributes and length of all files contained on the diskette. The system also provides facilities to format and backup diskettes.

"Wild card" commands are available for all file maintenance utilities. This allows the user to perform several functions with a single command. For example, to delete all files with an extension of BIN, the user would type "DELETE *. BIN.".

PROM Programmer

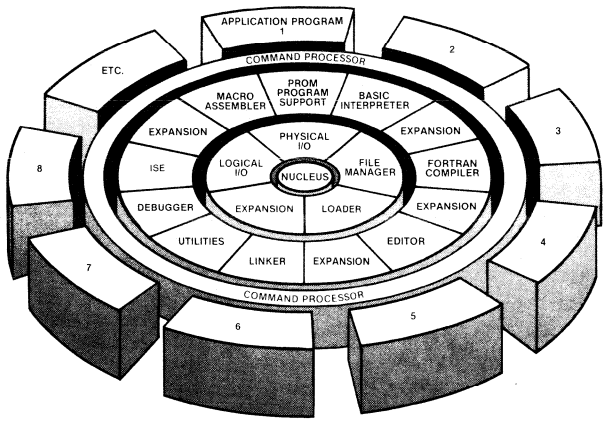
The PROM Programmer option provides a powerful and easy-to-use tool to program a wide range of PROM's. The PROM Programmer support system allows PROM code to be listed, verified and copied. When programming a PROM, the created code is written directly into the PROM mounted in the STARPLEX Development System PROM Programmer hardware. The source/destination for PROM data may be a PROM, diskette, memory, the video monitor or keyboard.

System Calls	
OPEN	Prepare file for access.
CLOSE	Update pointers and make file unavailable for access.
READ	Transfer a block or line of data from specified file to host memory and wait for completion.
READI	Begin to transfer a block or line of data from specified file to host memory and return control to caller.
WRITE	Transfer a block of data from host memory to specified file and wait for completion.
WRITEI	Begin to transfer a block of data from host memory to specified file and return control to caller.
DELETE	Remove file entry from directory and release file storage.
FPOS	Set or determine current position of a file pointer.
IOCHK	Check for completion of previous READI or WRITEI command.
IOWAIT	Wait for completion of previous READI, FPOS, or WRITE I command.
ATTRIB	Set or reset attributes of an opened file.
RENAME	Change name of a file in file directory.
DISKIO	Direct access to diskette without file management control.
EXIT	Normal return to operating system.
EREXIT	Abnormal return to operating system.
KBDMSK	Masks the availability of keyboard characters to a program.

Order Information

Included with the STARPLEX Development System, SPX-80/40 and SPX-80/40E.

STARPLEX™ BASIC



- **Extended Disc BASIC**
  - Powerful interactive language
  - Easy to use and understand
- **Language Extensions**
  - Enhance flexibility and capabilities
  - Provide memory management facilities
  - Direct access to memory and I/O ports
  - Extensive string operating capabilities
- **Supported by STARPLEX Disc Operating System**
  - Complete file management
  - Allocates and protects disc storage
- **Program Development Aids**
  - Minimize program development time

Product Overview

STARPLEX BASIC is an extension of the language originally developed at Dartmouth College. It provides a powerful, interactive programming language that can be used to solve a wide range of application problems. Because its instruction set resembles English statements, BASIC is easily understood and quickly learned.

Several additions to STARPLEX BASIC enhance the original language's capabilities and increase its flexibility. Among these enhancements are a complete set of data types, additional statements and functions, comprehensive data management facilities and multi-dimensional array capabilities.

STARPLEX BASIC is fully supported by the STARPLEX Disc Operating System. This allows the user to take advantage of the extensive operating system features including independent I/O and dynamically creating, accessing or deleting files. Data management features allow access to files created in any language supported by the operating system.

STARPLEX BASIC gives the programmer a wide variety of statements and commands that minimize program development time. For example, trace statements allow the execution of programs to be monitored, while edit facilities permit modifications to be made quickly and easily.

Functional Description

STARPLEX BASIC operates in 16K bytes of memory, and provides the user with a full range of arithmetic and relational operators, multi-dimensional arrays and mathematical functions.

STARPLEX BASIC combines features of an interpreter and a compiler. When a BASIC statement is entered from the keyboard, the program performs an immediate translation to a more compact format. This method makes more efficient use of memory than an interpreter but still permits the input source to be examined and modified.

Data Types

The following data types are supported:

- Integers (−32,768 to 32,767)
- Single Precision Floating Point (to 7 digits)
- Double Precision Floating Point (to 16 digits)
- Strings (to 255 characters)

Extensions

- Integer Division — forces arguments and quotient to integer form. It provides an operation to perform division which is eight times as fast as standard floating point.
- PEEK and POKE — allow a byte to be retrieved and stored at a specific memory location.
- INP and OUT — allow a byte to be read from or written to a specific port.
- ERASE — allows arrays to be eliminated and their space in memory used for other purposes.
- CONSOLE — allows the console terminal to be switched to a different I/O port.

Special Features

- Error Trapping — allows the user to override system error processing and write routines to handle error recovery or provide more complete error messages.
- String Operators — enable operations on ASCII character strings similar to numeric constants. For example, strings can be compared, moved or concatonated.
- Multi-Dimensional Arrays — provide the capability to define arrays with up to ten dimensions.
- Assembly Language Subroutines — can be called from BASIC programs.

Program Development Features

- Editing Facilities — permit the user to correct, add or delete individual characters or program lines.
- MERGE Command — allows parts of two programs to be put together to form a new program.
- Direct Mode — permits immediate execution of statements without writing a program. Statements are executed as they are entered and the results displayed for later use.
- Trace Commands — cause the line number of each line in the program to be printed as it is executed. The trace function can be turned on or off by the TRON and TROFF commands.
- RENUM Command — allows program lines, branches and calls to be re-sequenced to permit insertion of new lines. The programmer may specify the increment and line number range to be renumbered.

Statement Summary

CLOSE	Finish I/O to a particular data file
CONSOLE	Switch console terminal to another I/O port
DATA	Store a list of values in memory
DEF	Define a function
DIM	Allocate space for arrays
DSKF	Find free disc space
END	Terminate execution of program
ERASE	Eliminate arrays to reuse memory space
ERROR	Generate error code
FIELD	Associate a file's random buffer with a string variable
FOR . . . TO . . .	Loop control
GET	Read random file
GOSUB	Transfer to subroutine
GOTO	Unconditional branch
IF . . . GOTO . . .	Conditional branch
IF . . . THEN . . .	Conditional branch
INPUT	Read data from terminal or disc
KILL	Delete a file from the disc
LET	Assign a value to a variable
LSET	Insert string variable into random buffer
NAME	Rename file
NEXT	Loop control
ON . . . GOTO	Condition branch
ON . . . GOSUB	Conditional branch to subroutine
ONERROR GO TO	Error trapping
OPEN	Allow access to data file
OUT	Send a byte to an I/O port
POKE	Store a byte in specific location

PRINT	Print data
PRINT . . . USING	Print data using specific output format
PUT	Write random file
READ	Access data
REM	Insert remark
RESTORE	Re-read data
RESUME	Continue execution
RETURN	Return from subroutine
RSET	Insert string variable into random buffer
STOP	Stop program execution
SWAP	Exchange
WAIT	Monitor status of I/O ports

Function Summary

ABS(X)	Absolute value of X
ASC(X$)	ASCII value of first character
ATN(X)	Arctangent of X
CINT(X)	Convert X to integer
CSNG(X)	Convert X to single precision
CDBL(X)	Convert X to double precision
CHR$(I)	Return single character for ASCII I
COS(X)	Cosine of X
EXP(X)	Exponential
FIX(X)	Return truncated integer part of X
FRE(0)	Return amount of free memory space
HEX$(X)	Convert number to hexadecimal format string
INP(I)	Read byte from port I
INSTR	Search for pattern within a string
INT	Greatest integer < = X
LEFT$(X$,I)	Left justified substring
LEN(X$)	Length of string
LOG(X)	Natural log
LPOS(X)	Position of line printer head
MID$(X$,I,J)	Return specific portion of a string
OCT$(X)	String representing octal X
PEEK(I)	Read memory
POS(I)	Console cursor position
RIGHT$(X$,I)	Right justified substring
RND(X)	Random number
SGN(X)	Sign of X
SIN(X)	Sine of X
SPACE$(I)	Blank string
SPC(I)	Point blanks on terminal
SQR(X)	Square root of X
STR$(X)	Convert number to string
STRING$(I,J)	Return a string of ASCII code J
TAB(I)	Space to position I
TAN(X)	Tangent of X
USR(X)	Call user routine
VAL(X$)	Value of string
VARPTR(V)	Return address of V

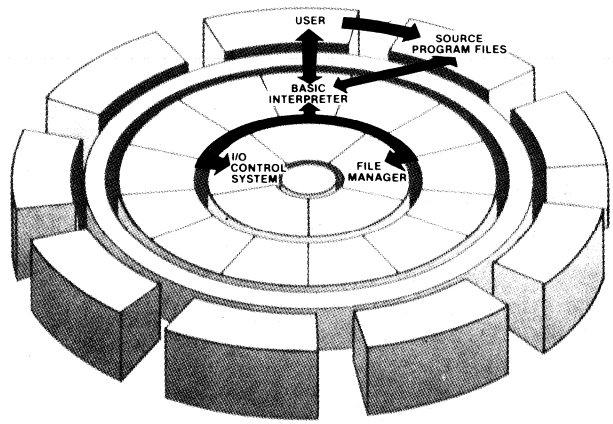
Command Summary

AUTO	Start automatic line numbering
CLEAR	Set all program variables to zero
CONT	Continue after CTRL/C, stop or error
DELETE	Delete a line or lines
EDIT	Edit a program line
FILES	Prints names of files residing on a diskette
LIST	List on console
LLIST	List on line printer
LOAD	Load a program from diskette
MERGE	Merge a source file from diskette into current program
MOUNT*	Allow access to drive
NEW	Delete current program and clear all variables
NULL	Set the number of null characters to be printed at end of each line
RENUM	Re-sequence line numbers
RUN	Run the program
SAVE	Save current program as source file on diskette
SYSTEM*	Return to STARPLEX system
TROFF	Turn off trace
TRON	Turn on trace
UNLOAD*	Close all open files and mark diskette as not mounted.
WIDTH	Set carriage width

*Note — May be used as a program statement.

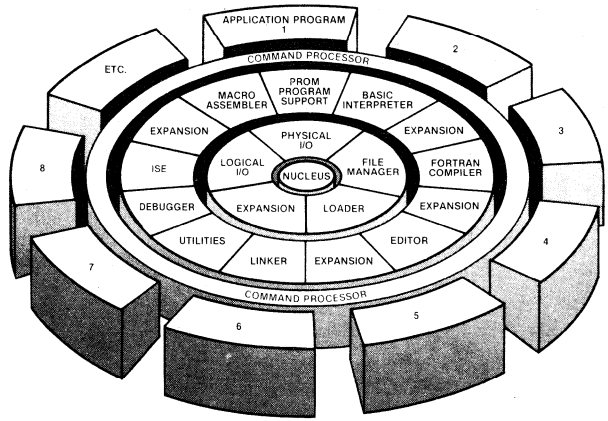
Order Information

Included with the STARPLEX Development System, SPX-80/40 and SPX-80/40E.



BASIC Interpreter-DOS System Diagram

STARPLEX™ FORTRAN IV



- **1966 ANSI Standard FORTRAN**
  - Programs are portable
  - Widely used language
- **Language Extensions**
  - Enhance flexibility and capabilities
  - Allow memory modification
  - Direct access to I/O ports
- **Supported by STARPLEX Disc Operating System**
  - Complete file management
  - Allocates and protects disc storage
- **User-Written I/O Drivers**
  - Non-standard devices easily interfaced
- **Extensive Library**
  - Single and Double Precision Data Types
  - Allows complex mathematical calculations

Product Overview

STARPLEX FORTRAN IV offers a widely-used, high-level language to the microcomputer user. It is a full implementation of the ANSI X3.9-1966 standard, with enhancements added to take advantage of the unique STARPLEX hardware features. Conformance to ANSI standards assures portability of existing FORTRAN programs.

Fully supported by the STARPLEX Disc Operating System, the user is provided with a complete I/O Control System and File Management facilities. These capabilities further enhance the flexibility of STARPLEX FORTRAN IV.

In addition to standard system I/O, STARPLEX FORTRAN IV allows the user to interface custom I/O drivers directly to FORTRAN programs, simplifying the task of accommodating non-standard devices.

STARPLEX FORTRAN IV offers an extensive subroutine library and supports double precision floating point data. These features enable the user to solve complex mathematical problems quickly.

Functional Description

The STARPLEX FORTRAN IV compiler is a one-pass translator which converts FORTRAN source statements into relocatable object modules. It can compile several hundred statements per minute

and needs less than 24K bytes of memory to compile most programs. The compiler optimizes the generated object code in several ways:

- Common Subexpression Elimination — Subexpressions are evaluated once and the value is substituted in later occurrences.
- Peephole Optimization — In special cases, such as I = I + 1, small sections of code are replaced by faster and more compact code.
- Constant Folding — Integer-constant expressions are evaluated at compile time.
- Branch Optimizations — In arithmetic and logical IF's the number of conditional jumps is minimized.
- Error Messages — Fully descriptive error messages and listings of the generated code are additional features of the compiler.

Enhancements

- One-Byte Variables — may be used as integer quantities in arithmetic expressions, as indices in DO loops, and in arrays, as string variables. This speeds calculations, adds flexibility and reduces memory requirements.
- Mixed Mode Arithmetic — allows variables of different types to be combined in arithmetic expressions.
- Hexadecimal Constants — may be defined and used whenever integer constants are normally allowed.
- Logical Operators — manipulate bits in one-byte variables.
- EOF and ERROR Condition Transfer — may be included with READ and WRITE statements to transfer control when an error or end-of-file condition is detected.
- ENCODE/DECODE Statements — provide easy conversion from integer or real numbers into character string or vice versa.
- Random Access Input/Output — allows a record number to be specified with disc READ or WRITE statements.

Operating System Support

STARPLEX FORTRAN IV is enhanced through both operating system and utility capabilities. The interactive STARPLEX Editor allows easy modification of both programs and data. The I/O Control System provides a central facility to process all I/O commands, permitting files created in FORTRAN to be used by BASIC and Assembler language programs.

All FORTRAN IV programs and subroutines are compiled into relocatable object modules. Each can be compiled separately, generating independent object modules. Subroutines may be placed in a system library to develop a common set of subroutines. The independent object modules can then be linked to create a run-time module. If the programmer wishes to change just one module of the program, only the changed module need be recompiled.

Customized I/O Drivers

All FORTRAN Input/Output operations are table-dispatched to the driver routine for the proper Logical Unit Number. To interface a non-standard device, the user writes a driver and updates the appropriate entry in the Logical Unit Number Table. This will cause all READ and WRITE statements specifying this Logical Unit Number to use the customized driver code.

FORTRAN Subroutine Library

The standard library of subroutines supplied with STARPLEX FORTRAN IV includes:

ABS
IABS
DABS

AINT
INT
IDINT

AMOD
MOD

AMAX0
AMAX1
MAX0
MAX1
DMAX1

AMIN0
AMIN1
MIN0
MIN1
DMIN1

FLOAT

IFIX

SIGN
ISIGN
DSIGN

DIM
IDIM

SNGL

DBLE

EXP
DEXP

ALOG
DLOG

ALOG10
DLOG10

SIN
DSIN

COS
DCOS

TANH

SQRT
DSQRT

ATAN
DATAN

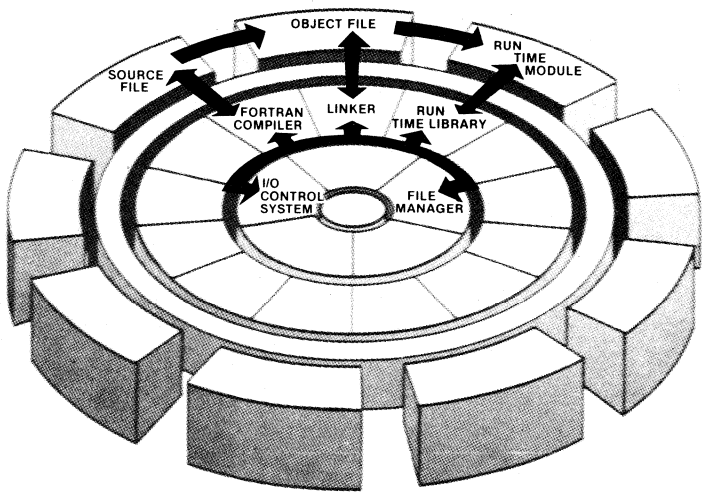
ATAN2
DTAN2

DMOD

In addition to the above list, four additional library routines — PEEK, POKE, INP and OUT are provided. PEEK and POKE allow direct access to any memory location. INP and OUT allow direct access to the I/O ports.

Comparison Table — ANSI vs STARPLEX FORTRAN IV

	FORTRAN	ANSI	STARPLEX FORTRAN
Data Type	Integer	Yes	Yes
	Real	Yes	Yes
	Double Precision	Yes	Yes
	Hollerith	Yes	Yes
	Logical (Byte)	No	Yes
Expressions	Arithmetic (+, −, *, /, **)	Yes	Yes
	Logical (NOT, AND, OR, XOR)	No	Yes
	Relational (LT, GT, LE, GE, EQ, NE)	Yes	Yes
	Mixed Mode	No	Yes
Input/Output Statements	READ/WRITE (formatted, unformatted)	Yes	Yes
	Random Access	No	Yes
	EOF and ERROR transfer	No	Yes
	ENCODE/DECODE	No	Yes
Non-executable Specifications	DIMENSION	Yes	Yes
	COMMON (blank, labeled)	Yes	Yes
	EQUIVALENCE	Yes	Yes
	EXTERNAL	Yes	Yes
	TYPE	Yes	Yes
	IMPLICIT	Yes	Yes
	DATA	Yes	Yes
	FORMAT	Yes	Yes
	BLOCK DATA	Yes	Yes
Control Statements	GO TO (unconditional & computed)	Yes	Yes
	IF (logical & arithmetic)	Yes	Yes
	CALL	Yes	Yes
	RETURN	Yes	Yes
	PAUSE	Yes	Yes
	STOP	Yes	Yes
	CONTINUE	Yes	Yes
	DO	Yes	Yes

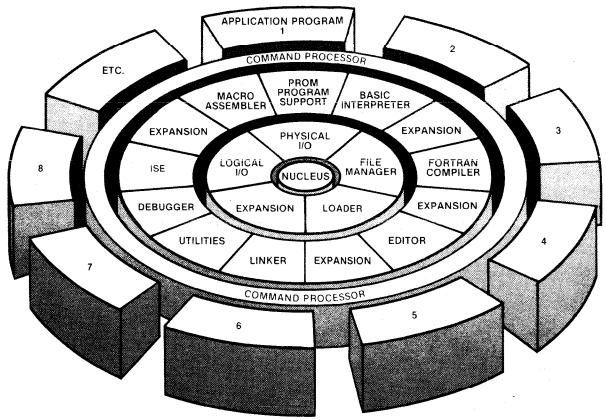


FORTRAN Compiler-DOS System Diagram

Order Information

Included with the Starplex Development System, SPX-80/40 and SPX-80/40E.

STARPLEX™ Editor



- **CRT-Oriented Editor**
  - Text always visible
  - Minimizes errors
- **Clearly Labeled Function Keys**
  - Eliminate complex command syntax
  - Simplify training
- **Forward and Backward Paging**
  - Provides review and correction capabilities
- **Automatic Source File Backup**
  - Protects files

Product Overview

The STARPLEX Editor is a general purpose tool for the creation and maintenance of ASCII text files. These files reside on a diskette formatted for operation on the STARPLEX System. Files created by the Editor may be used as input to the STARPLEX language processors or as general files.

The STARPLEX Editor provides a "friendly" interface between the user and the system. The novice will find it extremely easy to use, while the expert will appreciate its simplicity and flexibility. Instructions have been replaced by labeled function keys, making it unnecessary to remember or type commands. Training is simplified and errors caused by miskeyed instructions are eliminated.

Unlike line-oriented editors, the STARPLEX Editor never requires a line number or page position to be entered. Instead, an entire page of data and the cursor are displayed. If text is to be changed, the cursor is positioned and the appropriate function key struck. The display is constantly updated to reflect all corrections. By reviewing the text both before and after it is changed, the possibility of destroying data is minimized.

Functional Description

Text can be altered using one of three methods — type-over, insertion or deletion.

Type-over allows corrections to be made by positioning the cursor at the specific character and retyping it.

Deletions and insertions of either single characters or entire lines may be made; the Editor automatically creates or eliminates space as required.

Forward and backward paging permits continuous viewing of the data being edited. When all changes have been made, the entire file can be retrieved

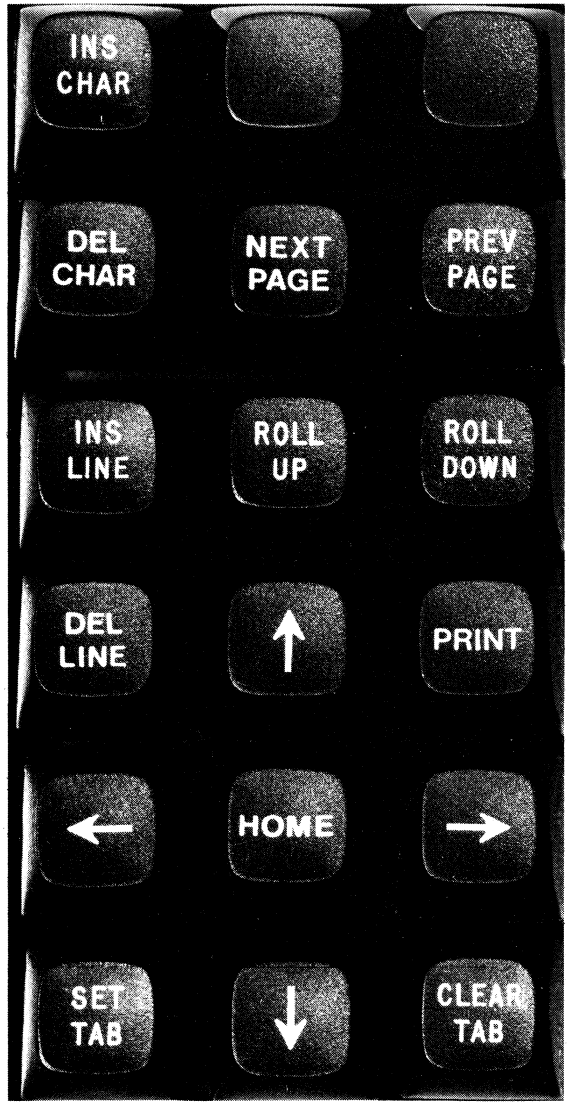
page-by-page for a final review and additional corrections made before leaving the Editor.

As the Editor is exited, the changes will be written to the disc file. To safeguard the original data, a backup file is automatically maintained.

The STARPLEX Editor is completely keystroke driven. If an ambiguous key is struck the Editor will signal with an audible tone and refuse to accept the implied command.

All keys are clearly labeled, and reference to an operator's manual is not necessary in order to use the STARPLEX Editor.

Editor Keypad

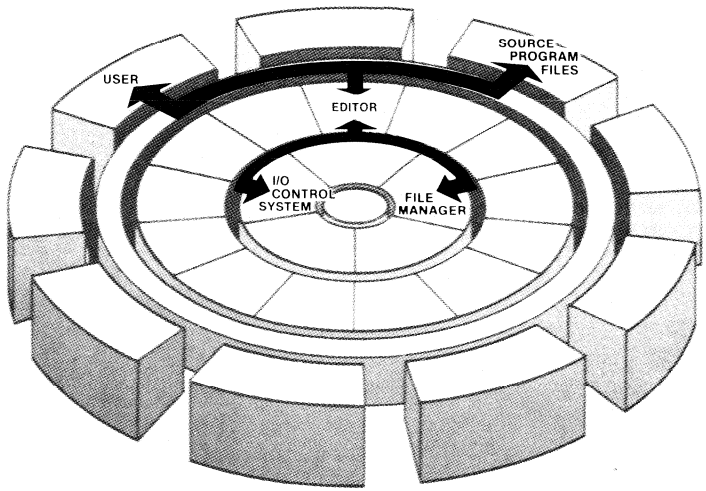


Key Description

PRINT	The CRT display is copied to the printer.
INS CHAR	The line is popped open at the cursor and the characters keyed are inserted.
INS LINE	A line of text is inserted.
DEL CHAR	The character at the cursor's position is deleted from the line.
DEL LINE	All characters from the cursor to the end of the current line are deleted.
ROLL UP	The screen is scrolled up one line.
ROLL DOWN	The screen is scrolled down one line.
PREV PAGE	The previous page of text is displayed on the CRT.
NEXT PAGE	The next page of text is displayed on the CRT.
↑	The cursor is moved up.
↓	The cursor is moved down.
→	The cursor is moved to the right.
←	The cursor is moved to the left.
HOME	The cursor is moved to the top left position on the screen.

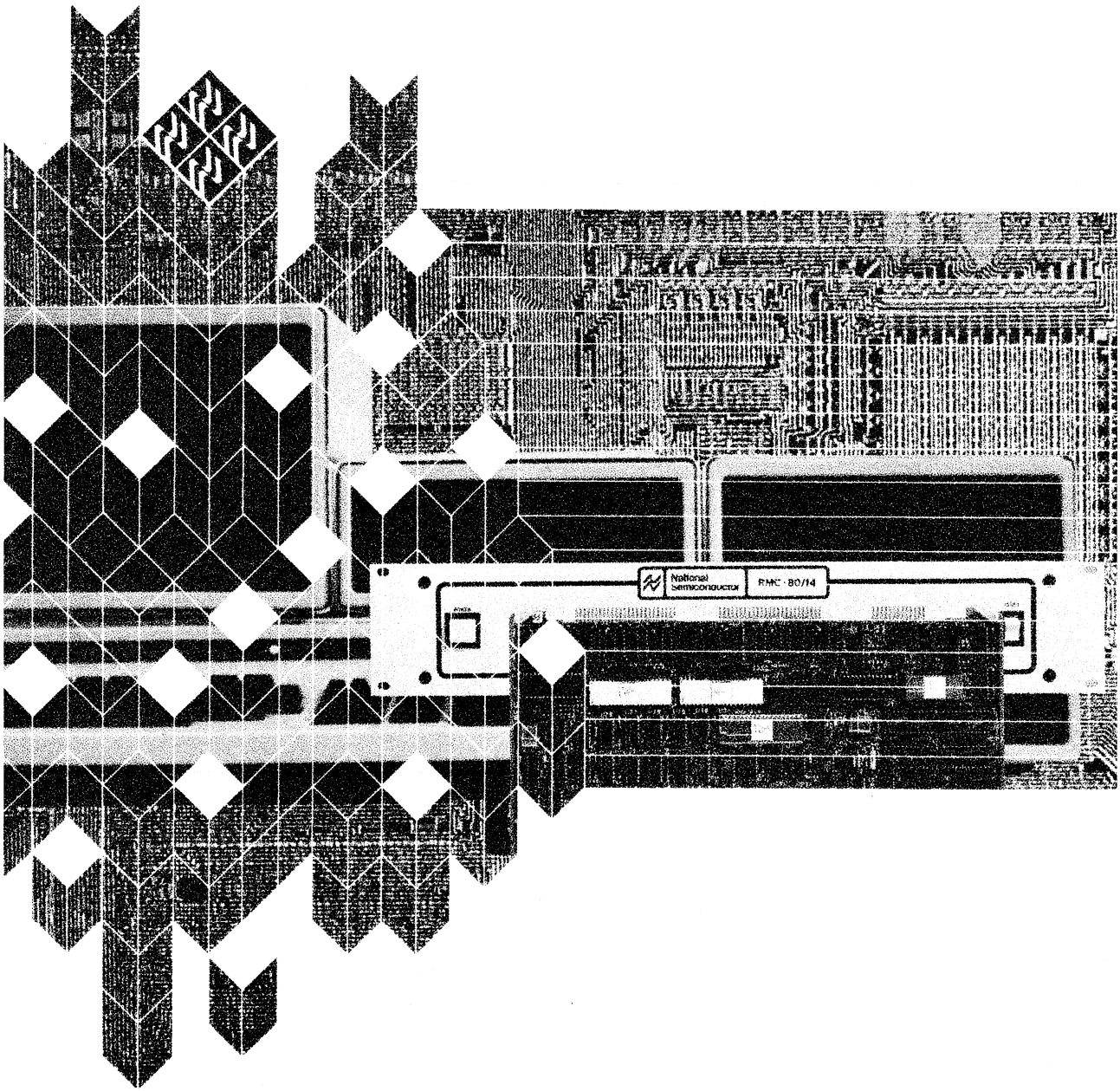
Order Information

Included with the STARPLEX Development System, SPX-80/40 and SPX-80/40E.



Editor-DOS System Diagram

Appendices



CPU Instructions

Appendix A

Mnemonic	Description	Execution Time (typical) Microseconds	
		BLC-80/07, 80/10, 80/11, 80/12, 80/14	BLC-80/204
DATA TRANSFER GROUP			
LDA	Load Accumulator Direct	6.34	6.05
LDAX B	Load Accumulator Indirect	3.42	3.26
LDAX D	Load Accumulator Indirect	3.42	3.26
LHLD	Load H and L Direct	7.81	7.44
LXI B	Load Immediate, Registers B and C	4.88	4.65
LXI D	Load Immediate, Registers D and E	4.88	4.65
LXI H	Load Immediate, Registers H and L	4.88	4.65
LXI SP	Load Immediate, Stack Pointer	4.88	4.65
MOV M,r	Move to Memory	3.42	3.26
MOV r,M	Move from Memory	3.42	3.26
MOV r1,r2	Move Registers	2.44	2.33
MVI M	Move to Memory Immediate	4.88	4.65
MVI r	Move Immediate	3.42	3.26
SHLD	Store H and L Direct	7.81	7.44
STA	Store Accumulator Direct	6.34	6.05
STAX B	Store Accumulator Indirect	3.42	3.26
STAX D	Store Accumulator Indirect	3.42	3.26
XCHG	Exchange H and L with D and E	1.95	1.86
ARITHMETIC GROUP			
ACI	Add Immediate with Carry	3.42	3.26
ADC M	Add Memory with Carry	3.42	3.26
ADC r	Add Register with Carry	1.95	1.86
ADD M	Add Memory	3.42	3.26
ADD r	Add Register	1.95	1.86
ADI	Add Immediate	3.42	3.26
DAA	Decimal Adjust Accumulator	1.95	1.86
DAD B	Add B and C to H and L	4.88	4.65
DAD D	Add D and E to H and L	4.88	4.65
DAD H	Add H and L to H and L	4.88	4.65
DAD SP	Add Stack Pointer to H and L	4.88	4.65
DCR M	Decrement Memory	4.88	4.65
DCR r	Decrement Register	2.44	2.33
DCX B	Decrement Registers B and C	2.44	2.33
DCX D	Decrement Registers D and E	2.44	2.33
DCX H	Decrement Registers H and L	2.44	2.33
DCX SP	Decrement Stack Pointer	2.44	2.33
INR M	Increment Memory	4.88	4.65
INR r	Increment Register	2.44	2.33
INX B	Increment Registers B and C	2.44	2.33
INX D	Increment Registers D and E	2.44	2.33
INX H	Increment Registers H and L	2.44	2.33
INX SP	Increment Stack Pointer	2.44	2.33
SBB M	Subtract Memory with Borrow	3.42	3.26
SBB r	Subtract Register with Borrow	1.95	1.86
SBI	Subtract Immediate with Borrow	3.42	3.26
SUB M	Subtract Memory	3.42	3.26
SUB r	Subtract Register	1.95	1.86
SUI	Subtract Immediate	3.42	3.26

CPU Instructions (continued)

Mnemonic	Description	Execution Time (typical) Microseconds	
		BLC-80/07, 80/10, 80/11, 80/12, 80/14	BLC-80/204
LOGICAL GROUP			
ANA M	AND Memory	3.42	3.26
ANA r	AND Register	1.95	1.86
ANI	AND Immediate	3.42	3.26
CMA	Complement Accumulator	1.95	1.86
CMC	Complement Carry	1.95	1.86
CMP M	Compare Memory	3.42	3.26
CMP r	Compare Register	1.95	1.86
CPI	Compare Immediate	3.42	3.26
ORA M	OR Memory	3.42	3.26
ORA r	OR Register	1.95	1.86
ORI	OR Immediate	3.42	3.26
RAL	Rotate Left through Carry	1.95	1.86
RAR	Rotate Right through Carry	1.95	1.86
RLC	Rotate Left	1.95	1.86
RRC	Rotate Right	1.95	1.86
STC	Set Carry	1.95	1.86
XRA M	Exclusive OR Memory	3.42	3.26
XRA r	Exclusive OR Register	1.95	1.86
XRI	Exclusive OR Immediate	3.42	3.26
BRANCH GROUP			
CALL	Call Unconditional	8.30	7.91
CC	Call on Carry	5.37/8.30	5.12/7.91
CM	Call on Minus	5.37/8.30	5.12/7.91
CNC	Call on No Carry	5.37/8.30	5.12/7.91
CNZ	Call on Not Zero	5.37/8.30	5.12/7.91
CP	Call on Positive	5.37/8.30	5.12/7.91
CPE	Call on Parity Even	5.37/8.30	5.12/7.91
CPO	Call on Parity Odd	5.37/8.30	5.12/7.91
CZ	Call on Zero	5.37/8.30	5.12/7.91
JC	Jump on Carry	4.88	4.65
JM	Jump on Minus	4.88	4.65
JMP	Jump Unconditional	4.88	4.65
JNC	Jump on No Carry	4.88	4.65
JNZ	Jump on Not Zero	4.88	4.65
JP	Jump on Positive	4.88	4.65
JPE	Jump on Parity Even	4.88	4.65
JPO	Jump on Parity Odd	4.88	4.65
JZ	Jump on Zero	4.88	4.65
PCHL	H and L to Program Counter	2.44	2.33
RC	Return on Carry	2.44/5.37	2.33/5.12
RET	Return	4.88	4.65
RM	Return on Minus	2.44/5.37	2.33/5.12
RNC	Return on No Carry	2.44/5.37	2.33/5.12
RNZ	Return on Not Zero	2.44/5.37	2.33/5.12
RP	Return on Positive	2.44/5.37	2.33/5.12
RPE	Return on Parity Even	2.44/5.37	2.33/5.12
RPO	Return on Parity Odd	2.44/5.37	2.33/5.12
RST	Restart	5.37	5.12
RZ	Return on Zero	2.44/5.37	2.33/5.12

CPU Instructions (continued)

Mnemonic	Description	Execution Time (typical) Microseconds	
		BLC-80/07, 80/10, 80/11, 80/12, 80/14	BLC-80/204
STACK, I/O, AND MACHINE CONTROL GROUP			
DI	Disable Interrupts	1.95	1.86
EI	Enable Interrupts	1.95	1.86
HLT	Halt	3.42	3.26
IN	Input	4.88	4.65
NOP	No Operation	1.95	1.86
OUT	Output	4.88	4.65
POP B	Pop Registers B and C off Stack	4.88	4.65
POP D	Pop Registers D and E off Stack	4.88	4.65
POP H	Pop Registers H and L off Stack	4.88	4.65
POP PSW	Pop Accumulator and Flags off Stack	4.88	4.65
PUSH B	Push Registers B and C on Stack	5.37	5.12
PUSH D	Push Registers D and E on Stack	5.37	5.12
PUSH H	Push Registers H and L on Stack	5.37	5.12
PUSH PSW	Push Accumulator and Flags on Stack	5.37	5.12
SPHL	Move H and L to Stack Pointer	2.44	2.33
XTHL	Exchange Top of Stack with H and L	8.78	8.37

Appendix B

Parallel Input/Output Control Parameters and Modes of Operation

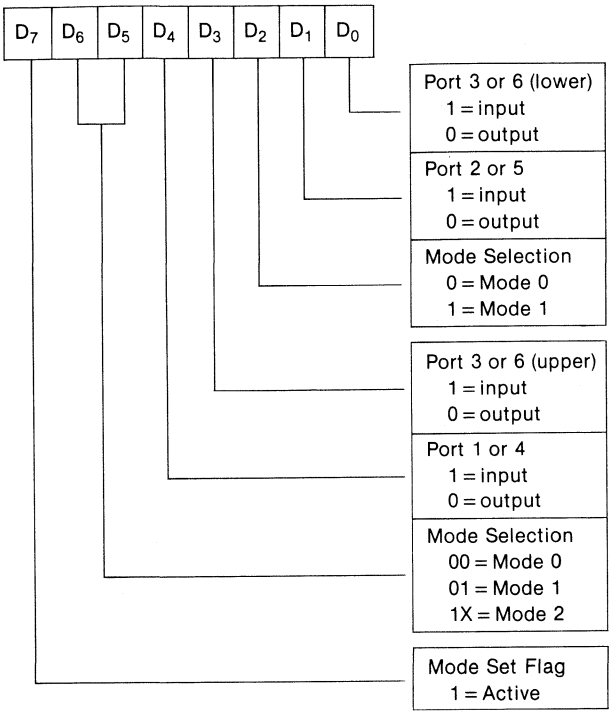
Port	No. of Lines	Input/Output		Unidirectional	Bidirectional	Control
		Unlatched	Latched and Strobed			
1	8	X	X	X	X	
2	8	X	X	X		
3	8	X		X		X

Input/Output Modes of Operation for the BLC-80/07

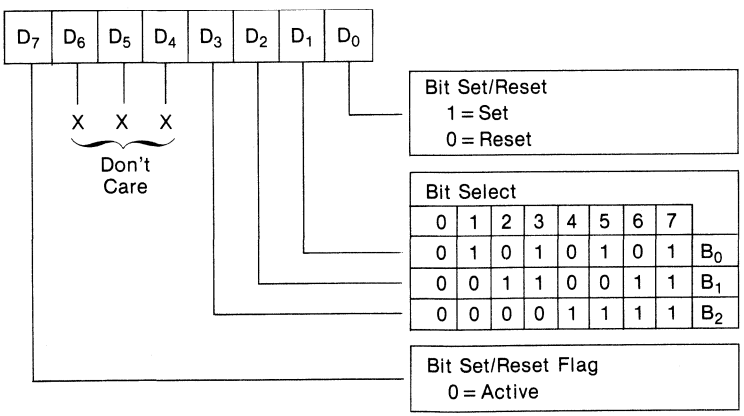
Port	No. of Lines	Mode of Operation					
		Unidirectional				Bidirectional	Control
		Input		Output			
		Unlatched	Latched and Strobed	Latched	Latched and Strobed		
1	8	X	X	X	X	X	
2	8	X	X	X	X		
3	8	X		X			X*
4	8	X		X			
5	8	X		X			
6	4	X		X			
	4	X		X			

*Mandatory when port 1 or port 2 is used in Latched & Strobed mode or port 1 is used in the bidirectional mode.

Input/Output Modes of Operation for the BLC-80/10, BLC-80/11, BLC-80/12, BLC-80/14, BLC-80/204, BLC-104, BLC-116, BLC-517



Mode Definition Control Word Format



Bit Set/Reset Control Word Format

National Semiconductor Corporation

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(408) 737-5000/TWX (910) 339-9240

DECEMBER 1978

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